**QDD-400COTU-5MCL**

**Features**

* Supports 425Gbps
* Single 3.3V Power Supply
* Power dissipation < 21W
* Up to 480km over SMF with EDFA
* RoHS compliant
* QSFP-DD MSA Compliant
* 8x53.125Gbps (PAM4) electrical interface
* Duplex LC connector
* Commercial case temperature range of 0°C to 70°C
* I2C interface with integrated Digital Diagnostic Monitoring
* Safety Certification: TUV/UL/FDA\*1
* RoHS compliant

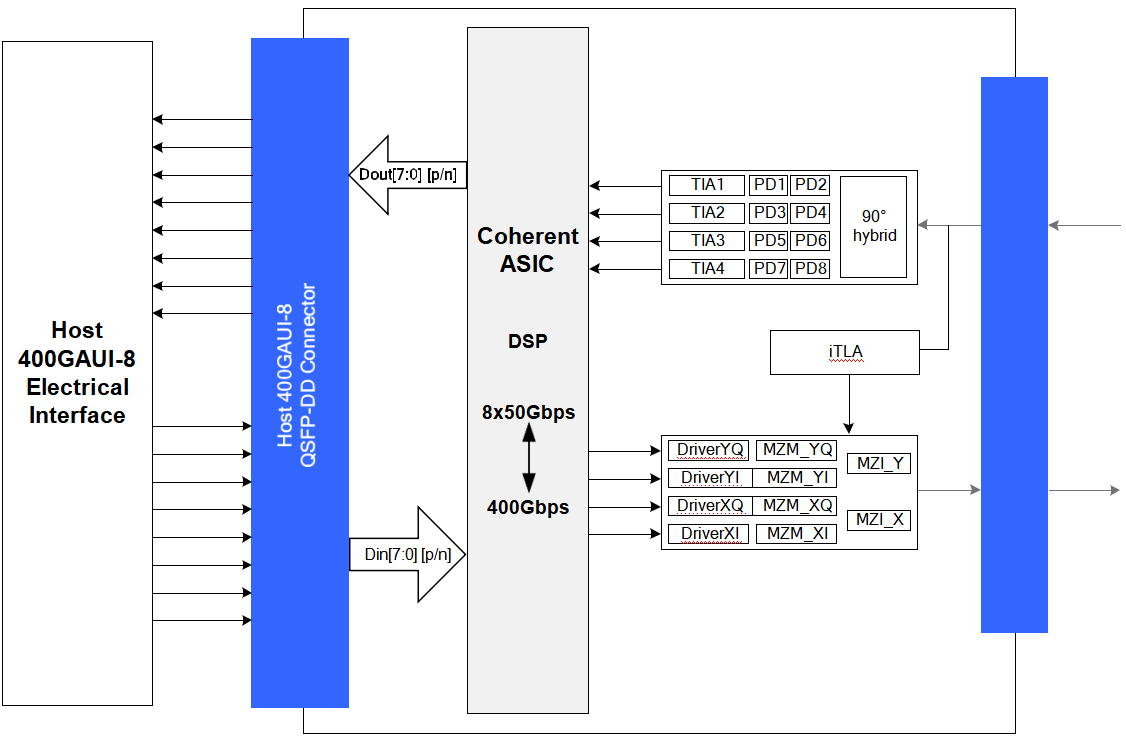
**Applications**

* 400G-ZR/ZR+ applications
* Data center interconnection
* DWDM networks

**Product Description**

AscentOptic’s QSFP-DD 400Gbps transceiver module is designed for optical communication applications in 400 Gigabit Ethernet links over 480km single mode fiber. This product converts 8 channels of 50 Gbps (PAM4) electrical input data to single channel of 400Gbps (DP-16QAM) coherent optical signals. Reversely, on the receiver side, 400Gbps (DP-16QAM) coherent optical signals is converted to 8 channels of 50Gbps (PAM4) electrical output data. The electrical interface of the module is compliant with the 400GAUI-8 interface as defined by IEEE 802.3bs, and the form factor, optical/electrical connection and digital diagnostic interface compliant with QSFP-DD MSA.

Figure 1: Transceiver Block Diagram



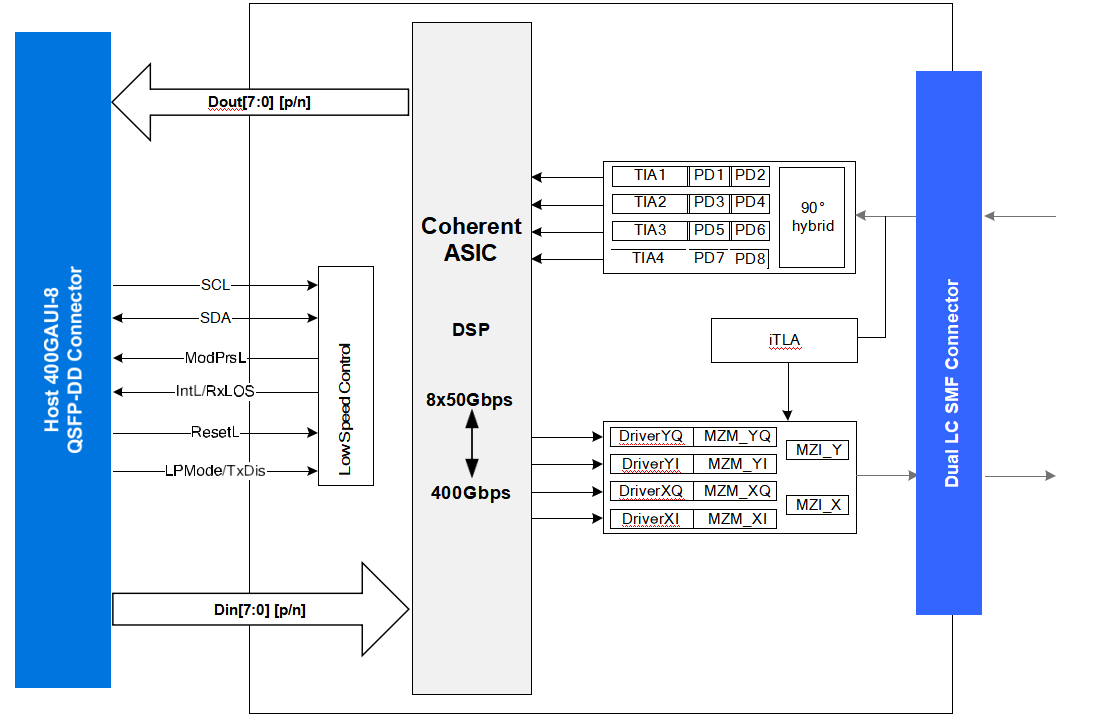


Figure 2: Application Reference Diagram

**Transmitter**

As shown in Figure 1, the transmitter path of the transceiver contains an 8x50Gbps 400GAUI-8 electrical input with equalization (EQ) block, integrated electrical multiplexer, iTLA, MZM and diagnostic monitor. The integrated electrical multiplexer converts 8 channels of 50 Gbps (PAM4) electrical input data to single channel of 400Gbps (DP-16QAM) optical signals.

**Receiver**

As shown in Figure 1, the receiver path of the transceiver contains eight PIN photodiodes, four trans- impedance amplifiers (TIA), integrated de-multiplexer and 8x50G 400GAUI-8 compliant electrical output blocks. The integrated de-multiplexer converts single channel of 400Gbps (DP-16QAM) optical signals to 8 channels of 50Gbps (PAM4) electrical output data.

**High Speed Electrical Signal Interface**

The interface between QSFP-DD module and ASIC/SerDes is shown in Figure 2. The high speed signal lines are internally AC-coupled and the electrical inputs are internally terminated to 100 Ohms differential. All transmitter and receiver electrical channels are compliant to module 400GAUI-8 specifications per IEEE 802.3bs.

**Control Signal Interface**

The control signal interface compliant with QSFP-DD MSA. The following pin are provided to control module or display the module status: ModPrsL, IntL/RxLOS, ResetL, LPMode/TxDis. In addition, there is an industry standard two wire serial interface scaled for 3.3 volt LVTTL. The definition of control signal interface and the registers of the serial interface memory are defined in the Control Interface & Memory Map section.

**Handling and Cleaning**

Exposure to current surges and over-voltage events can cause immediate damage to the transceiver module. Observe the precautions for normal operation of electrostatic discharge sensitive equipment; Attention shall also be paid to limiting transceiver module exposure to conditions beyond those specified in the absolute maximum ratings.

Optical connectors include female connectors. These elements will be exposed as long as the cable or port plug is not inserted. At this time, always pay attention to protection.

Each module is equipped with a port guard plug to protect the optical port. The protective plug shall always be in place whenever the optical fiber is not inserted. Before inserting the optical fiber, it is recommended to clean the end of the optical fiber connector to avoid contamination of the module optical port due to dirty connector. If contamination occurs, use standard LC port cleaning methods.

**Absolute Maximum Ratings**

Exceeding the absolute maximum ratings table may cause permanent damage to the device. This is just an emphasized rating, and does not involve the functional operation of the device that exceeds the specifications of this technical specification under these or other conditions. Long-term operation under absolute maximum ratings will affect the reliability of the device.

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Parameter** | **Symbol** | **Min.** | **Typical** | **Max.** | **Unit** |
| Storage Temperature | Ts | -40 |  | 85 | ℃ |

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Relative Humidity | RH | 5 |  | 85 | % |
| Power Supply Voltage | Vcc | -0.5 | 3.3 | 3.6 | V |
| Single Ended |  | -0.5 |  | Vcc+0.5 | V |
| Data Input Voltage |  |  |  |  |  |
| Differential\*5 |  |  |  | 0.8 | V |

**Note:**This is the maximum voltage that can be applied across the differential inputs without damaging the input circuitry. The damage threshold of the module input shall be at least 1600 mV peak to peak differential.

**Recommended Operating Conditions**

For operations beyond the recommended operating conditions, optical and electrical characteristics are not defined, reliability is not implied, and such operations for a long time may damage the module.

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Parameter** | **Symbol** | **Min.** | **Typical** | **Max.** | **Unit** |
| Operating Case Temperature\*7 | Tc | 0 |  | 70 | °C |
| Power Supply Voltage | Vcc | 3.135 | 3.3 | 3.465 | V |
| Power Supply Noise\*8 |  |  |  | 66 | mVpp |
| Power Dissipation | PD |  |  | 21 | W |
| Electrical Signal Rate Per Channel\*9 |  |  | 26.5625 |  | GBd |
| Optical Signal Rate Per Channel\*10 |  |  | 60.138546798 |  | GBd |
| Receiver Differential Data Output Load |  | 100 |  |  | Ohm |
| Fiber Length\*11 |  |  |  | 480 | km |

**Note:**

1. Power Supply specifications, Instantaneous, sustained and steady state current compliant with QSFP-DD MSA Power Classification.
2. The position of case temperature measurement is shown in Figure 9. Continuous operation at the maximum Recommended Operating Case Temperature should be avoided in order not to degrade reliability.
3. Power Supply Noise is defined as the peak-to-peak noise amplitude over the frequency range at the host supply side of the recommended power supply filter with the module and recommended filter in place. Voltage levels including peak-to- peak noise are limited to the recommended operating range of the associated power supply. See Figure 7 for recommended power supply filter.
4. 400GAUI-8 operation with Host generated FEC. The transmitter must receive pre-coded FEC signals from the host ASIC.
5. 400G ZR+ operation with Line generated OFEC.
6. 9μm SMF with EDFA.

**General Electrical Characteristics\*12**

Unless otherwise stated, the following characteristics are defined under recommended operating conditions.

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Parameter** | **Symbol** | **Min.** | **Typical** | **Max.** | **Unit** |
| Transceiver Power Consumption |  |  | 18 | 19 | W |
| Transceiver Power Supply Total Current |  |  | 6060 | 6670 | mA |
| AC Coupling Internal Capacitor |  |  | 0.1 |  | μF |

**Note**: For control signal timing including LPWn/PRSn, INT/RSTn, SCL and SDA see Control Interface Section.

**Reference Points**

|  |  |
| --- | --- |
| **Test Point** | **Description** |
| TP0 to TP5 | The channel including the transmitter and receiver differential controlled impedance |

|  |  |
| --- | --- |
|  | printed circuit board insertion loss and the cable assembly insertion loss. |
| TP1 to TP4 | All cable assembly measurements are made between TP1 and TP4 as illustrated in  Figure 3. |
| TP0 to TP2 TP3 to TP5 | A mated connector pair has been included in both the transmitter and receiver specifications defined in 802.3cd 136.9.3 and 136.9.4. The recommended maximum insertion loss from TP0 to TP2 or from TP3 to TP5 including the test fixture is provided  in 802.3cd 136.9.3.2 |
| TP2 | Unless specified otherwise, all transmitter measurements defined in 802.3cd 136.9.3  are made at TP2 utilizing the test fixture specified in Annex 136B. |
| TP3 | Unless specified otherwise, all receiver measurements and tests defined in 802.3cd  136.9.4 are made at TP3 utilizing the test fixture specified in Annex 136B. |



Figure 3: IEEE 802.3cd 50GBASE-CR, 100GBASE-CR2 or 200GBASE-CR4 link

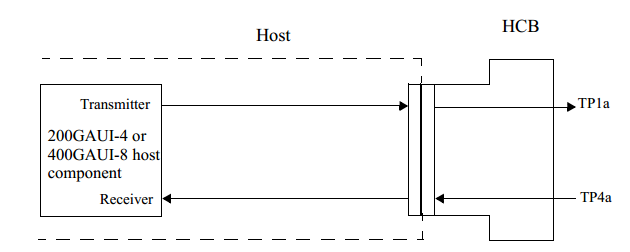


Figure 4: IEEE 802.3bs 400GAUI-8 compliance points TP1a, TP4a

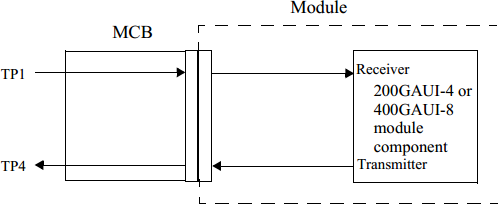


Figure 5: IEEE 802.3bs 400GAUI-8 compliance points TP1, TP4

**High Speed Electrical Input Characteristics**

Unless otherwise stated, the following characteristics are defined under recommended operating conditions.

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| **Parameter** | **Test Point** | **Min.** | **Typical** | **Max.** | **Unit** | **Conditions** |
| Signaling Rate, Per Lane  (PAM4 Encoded) | TP1 |  | 26.5625 |  | GBd | +/- 100 ppm |
| Differential Peak-Peak Input  Voltage Tolerance | TP1a | 900 |  |  | mV |  |
| Differential Input Return Loss  (Min) | TP1 |  | Equation  (83E-5) |  | dB | 802.3bs |
| Differential To Common  Mode Input Return Loss (Min) | TP1 |  | Equation (83E-6) |  | dB | 802.3bs |
| Differential Termination  Mismatch | TP1 |  |  | 10 | % |  |
| Single-Ended Voltage  Tolerance Range | TP1a | -0.4 |  | 3.3 | V |  |
| DC Common-Mode Output Voltage\*13 | TP1 | -350 |  | 2850 | mV |  |
| Module Stressed Input Test  \*14 |  |  |  |  |  |  |
| Eye Width |  |  | 0.22 |  | UI |  |
| Applied Peak-Peak  Sinusoidal Jitter |  |  | Table 120E-6 |  |  | 802.3bs |
| Eye Height |  |  | 32 |  | mV |  |

**Note:**

1. DC common mode voltage generated by the host. Specification includes effects of ground offset voltage.
2. Module stressed input tolerance is measured using the procedure defined in 120E.1.1.

**High Speed Electrical Output Characteristics**

Unless otherwise stated, the following characteristics are defined under recommended operating conditions.

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Parameter** | **Test Point** | **Min.** | **Typical** | **Max.** | **Unit** |
| Signaling Rate Per Lane(Range) | TP4a |  | 26.5625 ± 100  ppm |  | GBd |
| Differential Peak-To-Peak Input Voltage Tolerance | TP4 |  |  | 900 | mV |
| Differential Input Return Loss (Min) | TP4a |  | Equation(83E-5) |  | dB |
| Differential To Common Mode Input Return Loss (Min) | TP4a |  | Equation(83E-6) |  | dB |
| Differential Termination Mismatch | TP4a |  |  | 10 | % |
| Common Mode Voltage | TP4a | -0.35 |  | 2.85 | V |
| Transition time (20% to 80%) | TP4 | 9.5 |  |  | ps |

**High Speed Optical Transmitter Characteristics**

Unless otherwise stated, the following characteristics are defined under recommended operating conditions.

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Parameter** | **Symbol** | **Min.** | **Typical** | **Max.** | **Unit** |
| Signaling Speed |  | 60.138546798±20ppm | |  | GBd |
| Modulation format |  |  | DP-16QAM |  |  |
| Channel frequency | λ | 191.3 | 196.1 | | THz |
| Channel Spacing |  |  | 100(75) |  | GHz |
| Wavelength Accuracy |  | -1.8 |  | 1.8 | GHz |
| Tx Spectral Excursion |  | -32 |  | 32 | GHz |
| Average launch power |  | -10 |  | -6 | dBm |
| Output power with Tx disabled |  |  |  | -20 | dBm |
| Output power during wavelength  switching |  |  |  | -20 | dBm |
| In band OSNR |  | 34 |  | dB/0.1nm | |
| Out of band OSNR |  | 23 |  | dB/0.1nm | |
| Transmitter Reflectance |  |  |  | -20 | dB |
| Transmitter back reflectance  tolerance |  |  |  | -24 | dB |
| Transmitter polarization dependent  power |  |  |  | 1.5 | dBm |
| X-Y Skew |  |  |  | 5 | ps |
| DC I-Q offset(mean per  polarization) |  |  |  | -26 | dB |
| I-Q instantaneous offset |  |  |  | -20 | dB |
| Mean I-Q amplitude imbalance |  |  |  | 1 | dB |

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| I-Q phase imbalance | -5 |  | 5 |  | degrees |
| I-Q Skew(per polarization) |  |  | 0.75 |  | ps |
| Laser RIN(0.2GHz≤f≤10GHz Avg) |  |  | -145 |  | dB/Hz |
| Laser RIN(0.2GHz≤f≤10GHz Peak) |  |  | -140 |  | dB/Hz |
| Transmitter laser disable time |  |  | 100 |  | ms |
| Transmitter turn-up time from warm  start |  |  | 180 |  | s |
| Transmitter turn-up time from cold  start |  |  | 200 |  | s |
| Transmitter wavelength switching  time |  |  | 180 |  | s |
| Output power monitor Accuracy | -2 |  | 2 |  | dB |

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**High Speed Optical Receiver Characteristics**

Unless otherwise stated, the following characteristics are defined under recommended operating conditions.

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Parameter** | **Symbol** | **Min.** | **Typical** | **Max.** | **Unit** |
| Signaling Speed |  | 60.138546798±20ppm | |  | GBd |
| Channel frequency | λ | 191.3 |  | 196.1 | THz |
| Frequency offset between received  carrier and LO |  | -3.6 |  | 3.6 | GHz |
| Input power range |  | -12 |  | 13 | dBm |
| Input sensitivity\*15 | Sen | -12 |  |  | dBm |
| OSNR Tolerance |  |  |  | 24 | dB/0.1nm |
| Optical return loss |  | 20 |  |  | dB |
| CD Tolerance |  | 9600 |  |  | ps/nm |
| Optical path OSNR penalty tolerance |  |  |  | 0.5 | dB |
| PMD tolerance |  | 20 |  |  | ps |
| Peak PDL tolerance |  | 3.5 |  |  | dB |
| Tolerance to change in SOP |  | 50 |  |  | Krad/s |
| Optical input power transient  tolerance |  | -2 |  | 2 | dB |
| Receiver turn-up time from warm start |  |  |  | 10 | s |
| Receiver turn-up time from cold start |  |  |  | 200 | s |
| Intput power monitor Accuracy |  | -4 |  | 4 | dB |
| Optical Rx\_LOS Assert Threshold | LOSA | -20 |  |  | dBm |
| Optical Rx\_LOS Deassert Threshold | LOSD |  |  | -15 | dBm |
| Optical Rx\_LOS Hysteresis |  | 1 |  | 2.5 | dBm |

Note: Measured with conformance test signal at TP3 for the BER specified in Open ZR+ MSA clause.

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**Regulatory Compliance Issues**

Various standard and regulations apply to the EOLD-164HG-E-XX5 modules. These include eye-safety, Component Recognition, RoHS, ESD, EMC and Immunity. Please note the transmitter module is a Class 1 laser product. See Regulatory Compliance Table for details.

**Electrostatic Discharge (ESD)**

The AQDD-400COTU-5MCL is complies with the ESD requirements described in the Regulatory Compliance Table. However, in the normal processing and operation of optical transceiver, the following two types of situations need special attention.

Case I: Before inserting the transceiver into the rack meeting the requirements of QSFP-DD MSA, ESD preventive measures must be taken to protect the equipment. For example, the grounding wrist strap, workbench and floor should be used wherever the transceiver is handled.

Case II: After the transceiver is installed, the electrostatic discharge outside the chassis of the host equipment shall be within the scope of system level ESD requirements. If the optical interface of the transceiver is exposed outside the host equipment cabinet, the transceiver may be subject to equipment system level ESD requirements.

**Electromagnetic Interference (EMI)**

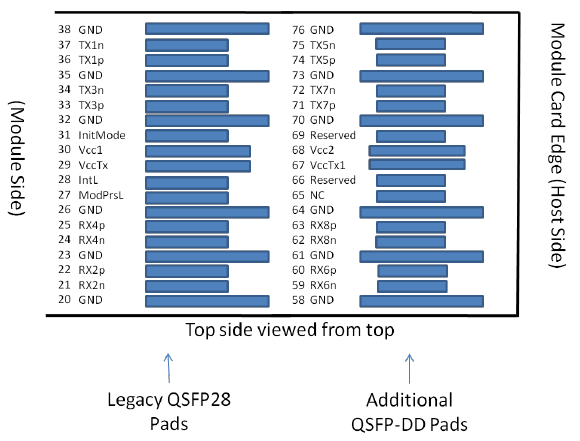
Communication equipment with optical transceivers is usually regulated by FCC in the United States and CENELEC EN55032 (CISPR 32) in Europe. The compliance of AQDD-400COTU-5MCL with these standards is detailed in the regulatory compliance table. The metal shell and shielding design of EOLD-164HG-E- XX5 will help equipment designers minimize the equipment level EMI challenges they face.

**Flammability**

AQSFPDD-400G-ZR-XYS optical transceiver meets UL certification requirements, its constituent materials have heat and corrosion resistance, and the plastic parts meet UL94V-0 requirements

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**QSFP-DD Transceiver Electrical Pad Layout**



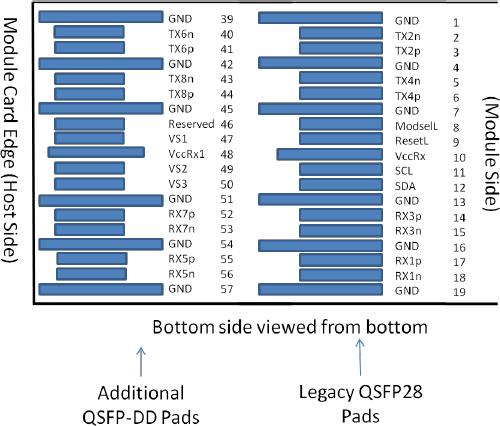


Figure 6: QSFP-DD Module Pinout

**Pin Arrangement and Definition**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Pin** | **Logic** | **Symbol** | **Description** | **Plug Sequence** | **Notes** |

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **1** |  | **GND** | **Ground** | **1B** | **1** |
| **2** | **CML-I** | **Tx2n** | **Transmitter Inverted Data Input** | **3B** |  |
| **3** | **CML-I** | **Tx2p** | **Transmitter Non-Inverted Data Input** | **3B** |  |
| **4** |  | **GND** | **Ground** | **1B** | **1** |
| **5** | **CML-I** | **Tx4n** | **Transmitter Inverted Data Input** | **3B** |  |
| **6** | **CML-I** | **Tx4p** | **Transmitter Non-Inverted Data Input** | **3B** |  |
| **7** |  | **GND** | **Ground** | **1B** | **1** |
| **8** | **LVTTL-I** | **ModSelL** | **Module Select** | **3B** |  |
| **9** | **LVTTL-I** | **ResetL** | **Module Reset** | **3B** |  |
| **10** |  | **VccRx** | **+3.3V Power Supply Receiver** | **2B** | **2** |
| **11** | **LVCMOS- I/O** | **SCL** | **2-wire serial interface clock** | **3B** |  |
| **12** | **LVCMOS- I/O** | **SDA** | **2-wire serial interface data** | **3B** |  |
| **13** |  | **GND** | **Ground** | **1B** | **1** |
| **14** | **CML-O** | **Rx3p** | **Receiver Non-Inverted Data Output** | **3B** |  |
| **15** | **CML-O** | **Rx3n** | **Receiver Inverted Data Output** | **3B** |  |
| **16** |  | **GND** | **Ground** | **1B** | **1** |
| **17** | **CML-O** | **Rx1p** | **Receiver Non-Inverted Data Output** | **3B** |  |
| **18** | **CML-O** | **Rx1n** | **Receiver Inverted Data Output** | **3B** |  |
| **19** |  | **GND** | **Ground** | **1B** | **1** |
| **20** |  | **GND** | **Ground** | **1B** | **1** |
| **21** | **CML-O** | **Rx2n** | **Receiver Inverted Data Output** | **3B** |  |
| **22** | **CML-O** | **Rx2p** | **Receiver Non-Inverted Data Output** | **3B** |  |
| **23** |  | **GND** | **Ground** | **1B** | **1** |
| **24** | **CML-O** | **Rx4n** | **Receiver Inverted Data Output** | **3B** |  |
| **25** | **CML-O** | **Rx4p** | **Receiver Non-Inverted Data Output** | **3B** |  |
| **26** |  | **GND** | **Ground** | **1B** | **1** |
| **27** | **LVTTL-O** | **ModPrsL** | **Module Present** | **3B** |  |
| **28** | **LVTTL-O** | **IntL** | **Interrupt** | **3B** |  |
| **29** |  | **VccTx** | **+3.3V Power supply transmitter** | **2B** | **2** |
| **30** |  | **Vcc1** | **+3.3V Power supply** | **2B** | **2** |
| **31** | **LVTTL-I** | **LPMode** | **Low Power Mode** | **3B** |  |
| **32** |  | **GND** | **Ground** | **1B** | **1** |
| **33** | **CML-I** | **Tx3p** | **Transmitter Non-Inverted Data Input** | **3B** |  |
| **34** | **CML-I** | **Tx3n** | **Transmitter Inverted Data Input** | **3B** |  |
| **35** |  | **GND** | **Ground** | **1B** | **1** |
| **36** | **CML-I** | **Tx1p** | **Transmitter Non-Inverted Data Input** | **3B** |  |
| **37** | **CML-I** | **Tx1n** | **Transmitter Inverted Data Input** | **3B** |  |
| **38** |  | **GND** | **Ground** | **1B** | **1** |
| **39** |  | **GND** | **Ground** | **1A** | **1** |
| **40** | **CML-I** | **Tx6n** | **Transmitter Inverted Data Input** | **3A** |  |
| **41** | **CML-I** | **Tx6p** | **Transmitter Non-Inverted Data Input** | **3A** |  |
| **42** |  | **GND** | **Ground** | **1A** | **1** |
| **43** | **CML-I** | **Tx8n** | **Transmitter Inverted Data Input** | **3A** |  |
| **44** | **CML-I** | **Tx8p** | **Transmitter Non-Inverted Data Input** | **3A** |  |
| **45** |  | **GND** | **Ground** | **1A** | **1** |
| **46** |  | **Reserved** | **For future use** | **3A** | **3** |
| **47** |  | **VS1** | **Module Vendor Specific 1** | **3A** | **3** |
| **48** |  | **VccRx1** | **3.3V Power Supply** | **2A** | **2** |
| **49** |  | **VS2** | **Module Vendor Specific 2** | **3A** | **3** |
| **50** |  | **VS3** | **Module Vendor Specific 3** | **3A** | **3** |
| **51** |  | **GND** | **Ground** | **1A** | **1** |
| **52** | **CML-O** | **Rx7p** | **Receiver Non-Inverted Data Output** | **3A** |  |
| **53** | **CML-O** | **Rx7n** | **Receiver Inverted Data Output** | **3A** |  |
| **54** |  | **GND** | **Ground** | **1A** | **1** |
| **55** | **CML-O** | **Rx5p** | **Receiver Non-Inverted Data Output** | **3A** |  |
| **56** | **CML-O** | **Rx5n** | **Receiver Inverted Data Output** | **3A** |  |
| **57** |  | **GND** | **Ground** | **1A** | **1** |
| **58** |  | **GND** | **Ground** | **1A** | **1** |
| **59** | **CML-O** | **Rx6n** | **Receiver Inverted Data Output** | **3A** |  |
| **60** | **CML-O** | **Rx6p** | **Receiver Non-Inverted Data Output** | **3A** |  |
| **61** |  | **GND** | **Ground** | **1A** | **1** |
| **62** | **CML-O** | **Rx8n** | **Receiver Inverted Data Output** | **3A** |  |
| **63** | **CML-O** | **Rx8p** | **Receiver Non-Inverted Data Output** | **3A** |  |
| **64** |  | **GND** | **Ground** | **1A** | **1** |
| **65** |  | **NC** | **No Connect** | **3A** | **3** |
| **66** |  | **Reserved** | **For future use** | **3A** | **3** |
| **67** |  | **VccTx1** | **3.3V Power Supply** | **2A** | **2** |
| **68** |  | **Vcc2** | **3.3V Power Supply** | **2A** | **2** |
| **69** |  | **Reserved** | **For Future Use** | **3A** | **3** |
| **70** |  | **GND** | **Ground** | **1A** | **1** |
| **71** | **CML-I** | **Tx7p** | **Transmitter Non-Inverted Data Input** | **3A** |  |
| **72** | **CML-I** | **Tx7n** | **Transmitter Inverted Data Input** | **3A** |  |
| **73** |  | **GND** | **Ground** | **1A** | **1** |
| **74** | **CML-I** | **Tx5p** | **Transmitter Non-Inverted Data Input** | **3A** |  |
| **75** | **CML-I** | **Tx5n** | **Transmitter Inverted Data Input** | **3A** |  |
| **76** |  | **GND** | **Ground** | **1A** | **1** |

|  |
| --- |
| 1: QSFP-DD uses common ground (GND) for all signals and supply (power). All are common within the QSFP-DD module and all module voltages are referenced to this potential unless otherwise noted.  Connect these directly to the host board signal-common ground plane. |
| 2: VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 shall be applied concurrently. VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 may be internally connected within the module in any combination. The  connector Vcc pins are each rated for a maximum current of 1000 mA. |
| 3: All Vendor Specific, Reserved and No Connect pins may be terminated with 50 ohms to ground on the host. Pad 65 (No Connect) shall be left unconnected within the module. Vendor specific and  Reserved pads shall have an impedance to GND that is greater than 10 k Ohms and less than 100 pF. |
| 4: Plug Sequence specifies the mating sequence of the host connector and module. The sequence is  1A, 2A, 3A, 1B, 2B, 3B. Contact sequence A will make, then break contact with additional QSFP-DD pads. Sequence 1A, 1B will then occur simultaneously, followed by 2A, 2B, followed by 3A, 3B. |

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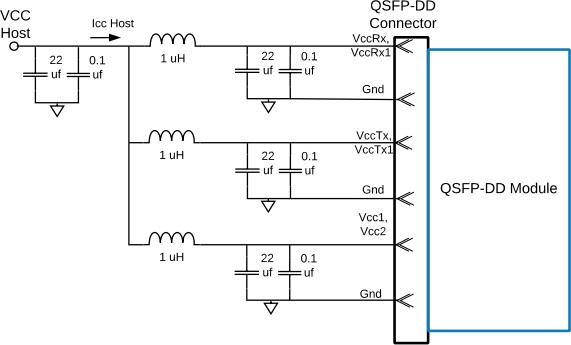


Figure 7: Host Board Power Supply Filter

During power transient events, the host should ensure that any neighboring modules sharing the same supply stay within their specified supply voltage limits. The host should also ensure that the intrinsic noise of the power rail is filtered in order to guarantee the correct operation of the optical modules. The reference power supply filter is shown in Figure 7.

**Package Outline**

The module is designed to meet the package outline defined in the QSFP-DD MSA specification. See the package outline for details.

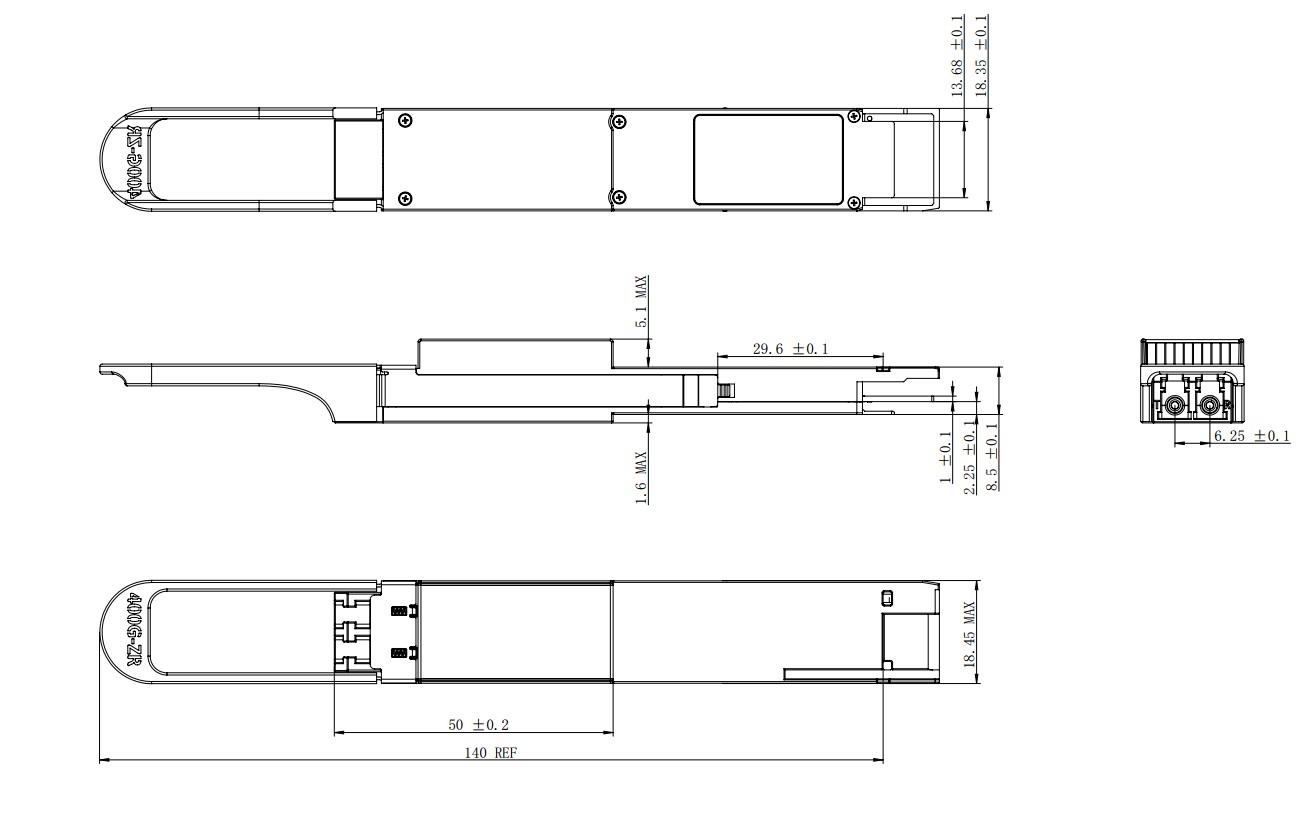


Figure 8: Mechanical Package Outline (All dimensions in mm)

\*This 2D drawing is only for reference, please check with Eoptolink before ordering.

The bellow picture shows the location of the hottest spot for measuring module case temperature. In addition, the digital diagnostic monitors (DDM) temperature is also calibrated to this spot

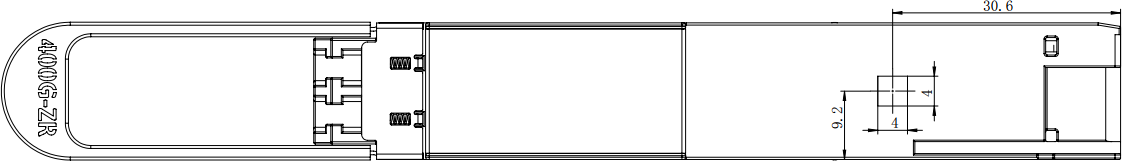


Figure 9: Case Temperature Measurement Point (All dimensions in mm)

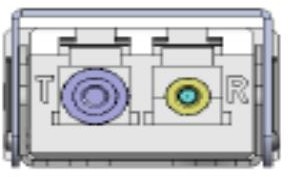
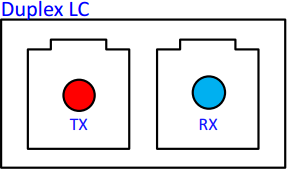
The optical interface port is a male Duplex LC connector as specified iTIA-604-10.

Figure 10: Module Optical Interface (looking into the optical port)

**Control Interface & Memory Map**

The control interface combines dedicated signal lines for ModeSelL, ResetL, LPMode/TxDis, ModPrsL, IntL/RxLOS with two-wire serial (TWS), interface clock (SCL) and data (SDA), signals to provide users rich functionality over an efficient and easily used interface.

# SCL and SDA

The SCL and SDA is a hot plug interface that may support a bus topology. During module insertion or removal, the module may implement a pre- charge circuit which prevents corrupting data transfers from other modules that are already using the bus.

# ModSelL

The ModSelL is an input signal that shall be pulled to Vcc in the QSFP-DD modules. When held low by the host, the module responds to TWI serial communication commands. The ModSelL allows the use of multiple QSFP-DD modules on a single TWI interface bus. When ModSelL is “High”, the module shall not respond to or acknowledge any TWI interface communication from the host.

In order to avoid conflicts, the host system shall not attempt TWI interface communications within the ModSelL de-assert time after any QSFP-DD modules are deselected. Similarly, the host must wait at least for the period of the ModSelL assert time before communicating with the newly selected module. The assertion and de-asserting periods of different modules may overlap as long as the above timing requirements are met.

# ResetL

The ResetL signal shall be pulled to Vcc in the module. A low level on the ResetL signal for longer than the minimum pulse length (t\_Reset\_init) initiates a complete module reset, returning all user module settings to their default state.

# LPMode/TxDis

LPMode/TxDis is a dual-mode input signal from the host operating with active high logic. It shall be pulled towards Vcc in the module. At power-up or after ResetL is deasserted LPMode/TxDis behaves as LPMode. If supported, LPMode/TxDis can be configured as TxDis using the TWI interface except during the execution of a reset. LPMode is used in the control of the module power mode.

When LPMode/TxDis is configured as LPMode, the module behaves as though TxDis=0. By using the LPMode signal and a combination of the Power\_override, Power\_set and High\_Power\_Class\_Enable software control bits the host controls how much power a module can consume. When LPMode/TxDis is configured as TxDis, the module behaves as though LPMode=0.

Changing LPMode/TxDis mode from LPMode to TxDis when the LPMode/TxDis state is high disables all optical transmitters. If the module was in low power mode, then the module transitions out of low power mode at the same time. If the module is already in high power state (Power Override control bits) with transmitters already enabled, the module shall disable all optical transmitters. Changing the LPMode/TxDis mode from LPMode to TxDis when the LPMode/TxDis state is low, simply changes the behavior of the mode of LPMode/TxDis. The behavior of the module depends on the Power Override control bits.

# ModPrsL

ModPrsL shall be pulled up to Vcc Host on the host board and pulled low in the module. The ModPrsL is asserted “Low” when the module is inserted. The ModPrsL is deasserted “High” when the module is physically absent from the host connector due to the pull-up resistor on the host board.

# IntL/RxLOSL

IntL/RxLOSL is a dual-mode active-low, open-collector output signal from the module. It shall be pulled up towards Vcc on the host board. At power-up or after ResetL is released to high, IntL/RxLOSL is configured as IntL. When the IntL signal is asserted Low it indicates a change in module state, a possible module operational fault or a status critical to the host system. The host identifies the source of the interrupt using the TWI serial interface. The IntL signal is deasserted “High” after all set interrupt flags are read. If dual mode operation supported, IntL/RxLOSL can be optionally programmed as RxLOSL using the TWI interface except during the execution of a reset. If the module has no interrupt flags asserted (IntL/RxLOSL is high), there should be no change in IntL/RxLOSL states after the mode change.

If IntL/RxLOSL is configured as RxLOSL, a low indicates that there is a loss of received optical power on at least one lane. “High” indicates that there is no loss of received optical power. The actual condition of loss of optical receive power is specified by other governing documents, as the alarm threshold level is application specific. The module shall pull RxLOSL to low if any lane in a multiple lane module or cable has a LOS condition and shall release RxLOSL to high only if no lane has a LOS condition.

**Low Speed Control and Sense Signals**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Parameter | Symbol | Min. | Typical | Max. | Unit |
| SCL and SDA | VOL | 0 |  | 0.4 | V |
| VOH | VCC-0.5 |  | VCC+0.3 | V |  |
| SCL and SDA | VIL | -0.3 |  | VCC\*0.3 | V |
| VIH | VCC\*0.7 |  | VCC+0.5 | V |  |
| LPMode/TxDis, ResetL, ModSelL | VIL | -0.3 |  | 0.8 | V |

**Memory Map**

The control interface and memory map of the QSFP-DD module is compliant with the QSFP-DD MSA. The QSFP-DD module support I2C interface protocol defined by the QSFP-DD MSA. Access clock frequency support a minimum of 100 kHz with no clock stretching.

1. The module initialize in hardware mode when LPMode is de-asserted.

2. The transmitter is disabled when the module is held in reset.

3. Tx and Rx squelch function are implemented as defined by the QSFP-DD MSA.

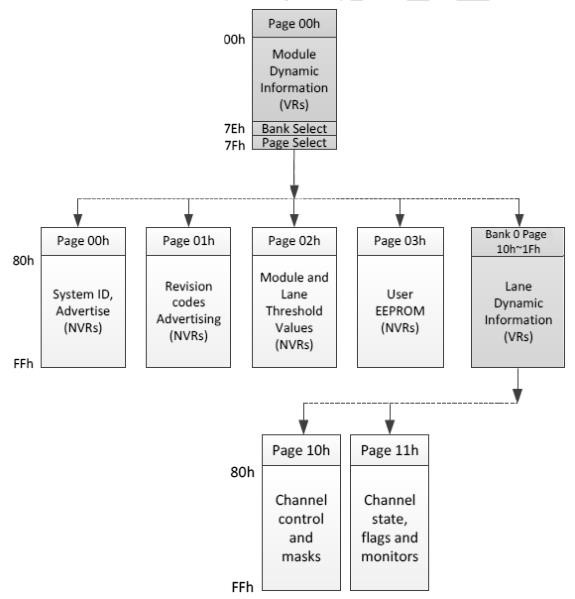
.

Figure 11: Simplified QSFP-DD CMIS Module Memory Map Architecture

**Ordering Information**

|  |  |
| --- | --- |
| **Part Number** | **Product Description** |
| QDD-400COTU-5MCL | 400Gbps, SMF , 480KM, Duplex LC, 0~70℃, with DDM |

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