400G-ZR QSFP-DD Optical Transceiver Module

QSFP-DD-400G-ZR

Table of Contents

List of tables:

1.1 General Description

The QSFP-DD-400G-ZR coherent module is designed for use in Data center interconnections (DCIs) links over single mode fiber. Compliant with the OIF 400ZR MSA and QSFP-DD MSA standards. Digital diagnostics functions are available via an I2C interface, as specified by the QSFP-DD MSA.

The QSFP-DD-400G-ZR is a C-Band 75G/100GHz grid coherent optical module, combines coherent DSP ASIC functionality with best in class ultra-narrow line-width tunable lasers, high speed modulators and high responsively coherent receivers to deliver high performance at 400G 16QAM modulation formats (at 60G baud rate).

Mechanical dimensions, connectors and footprint of QSFP-DD-400G-ZR conform to QSFP-DD MSA. The module is QSFP-DD type2 size, 18.4 mm x 93.4mm x 8.5mm and hot pluggable by 76-pin connector. The maximum power consumption is 16.5W and power supply voltage is +3.3V.

The functional block diagram is shown as below.

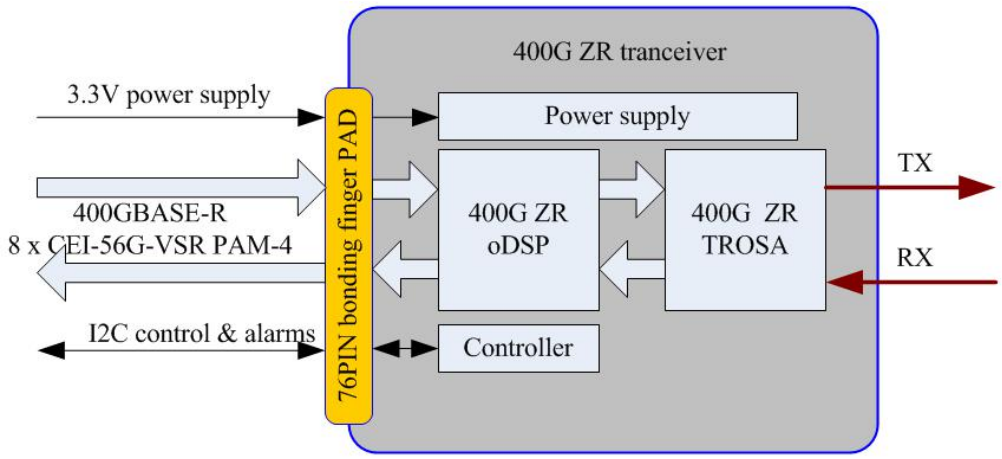


Figure 1 QSFP-DD-400G-ZR functional block diagram QSFP-DD-400G-ZR module designed for 400ZR type 1(code 0x01), Amplified application.

Table 1: Module Code

Module Code	Application	Reach
QSFP-DD-400G-ZR	Amplified	80-120km

1.2 Typical Application

1.3 QSFP-DD-400G-ZR is intended to be used in conjunction with a host platform to support 400G transmission over optical links in DCI applications, below is the reference diagram.

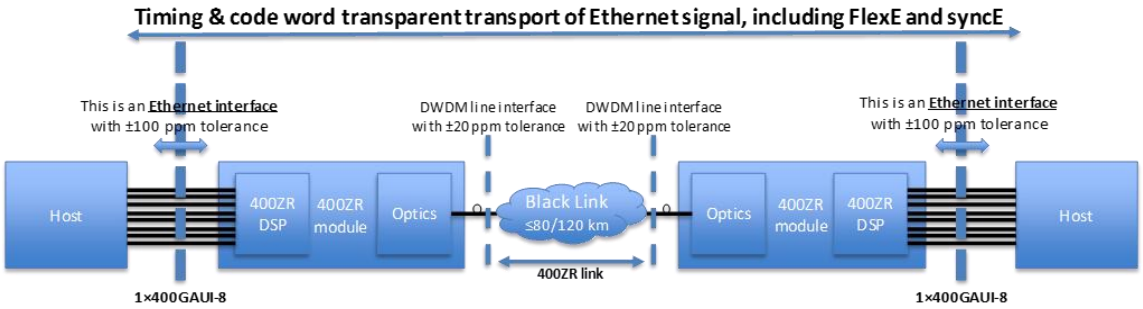


Figure 2 400ZR reference diagram

400ZR is identified for use in the following applications. The Module is target for Amplified point-to-point applications:

3 use cases of amplified point-to-point are identified for 400ZR. For amplified links the reach is dependent on the OSNR (noise limited) at the receiver. The 400ZR targeted reach for these applications is 80-120km or more.

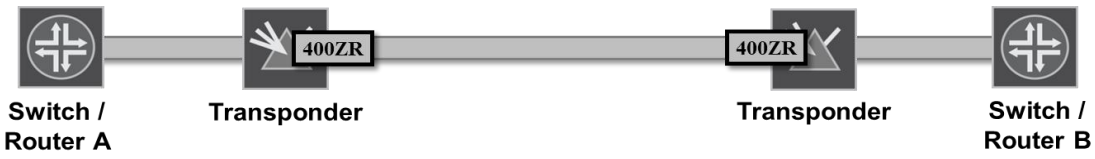


Figure 3 Transponder Line card with 400ZR amplified point to point interface

Figure 4 Router switch line card with 400ZR DWDM Interfaces

Figure 5 Transponder Line Card with 400ZR DWDM interfaces

1.4 Product Features

- QSFP-DD MSA compliant
- Compliant to OIF 400ZR, Version 01.0, March 10,2020
- Digital diagnostic monitoring support
- Hot pluggable 76 pin electrical interface
- Maximum power consumption 16.5W
- Supports 400G 16QAM Modulation
- Compact size (18.4 mm x 93.4mm x 8.5mm)
- LC duplex connector
- Support 400GBASE-R, 425Gb/s bit rate
- Support 400G-AUI-8 C2M; 8 x CEI-56G-VSR PAM-4 electrical interface
- Operating case temperature: 0 to 70 ℃
- Single 3.3V power supply
- RoHS 2.0 compliant

2 Environmental Specifications

The table below defines the environmental specifications of the QSFP-DD-400G-ZR module.
Note: Operating or handling the module out of any specified absolute maximum rating is subject to permanent damage of the module.

Table 2: Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Unit	Note
Power Supply Voltage	Vcc	-0.3	3.3	3.6	V	
Storage Temperature	Ts	-40		85	℃	
Relative Humidity	RH	15		85	%	Non-condensing
Receiver Damage Threshold	PRdmg	3			dBm	

Table 3: Operating Environments

Parameter	Symbol	Min	Typ	Max	Unit	Note
Case Temperature	Top	0		70	℃	

3.1 Recommended Operating Conditions

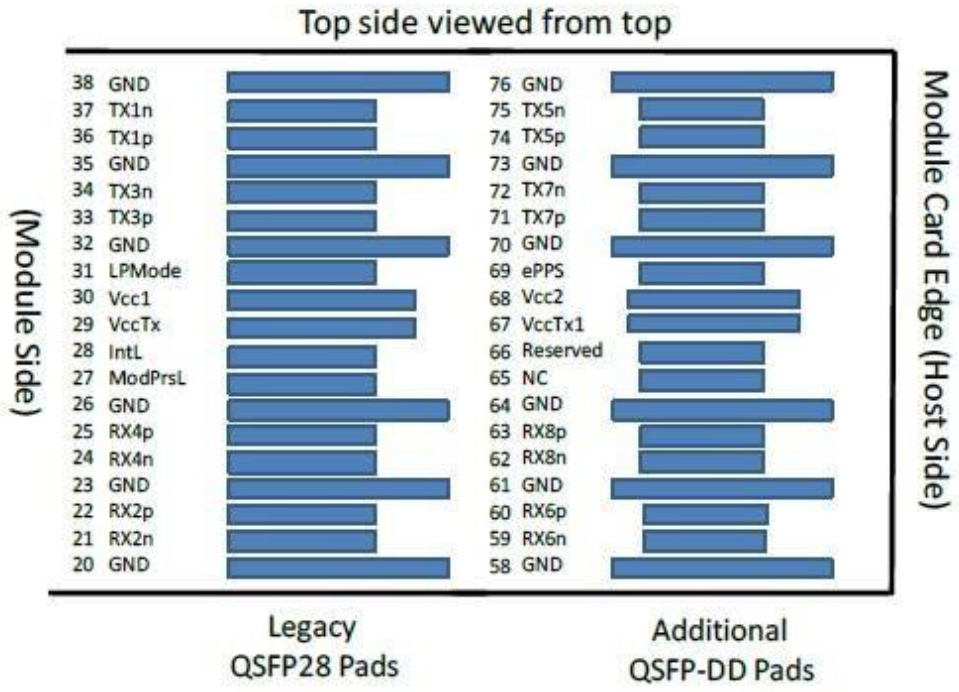
Table 4: Recommended Operating Conditions

Parameter	Symbol	Min	Typ.	Max	Unit	Note
Supply Voltage	Vcc	3.2	3.3	3.4	V	
Supply Current	Icc			5.2	A	Steady state
Power Supply Noise	Vrip			2 3	%	DC-1MHz 1-10MHz
Module Power consumption	Pcc			16.5	W	Power Class 8

Notes: Maximum total power value is specified across the full temperature(0℃-70℃) and voltage range(3.2V-3.4V).

3.2 Host Electrical Connector & Pin Assignments

Module pad layout



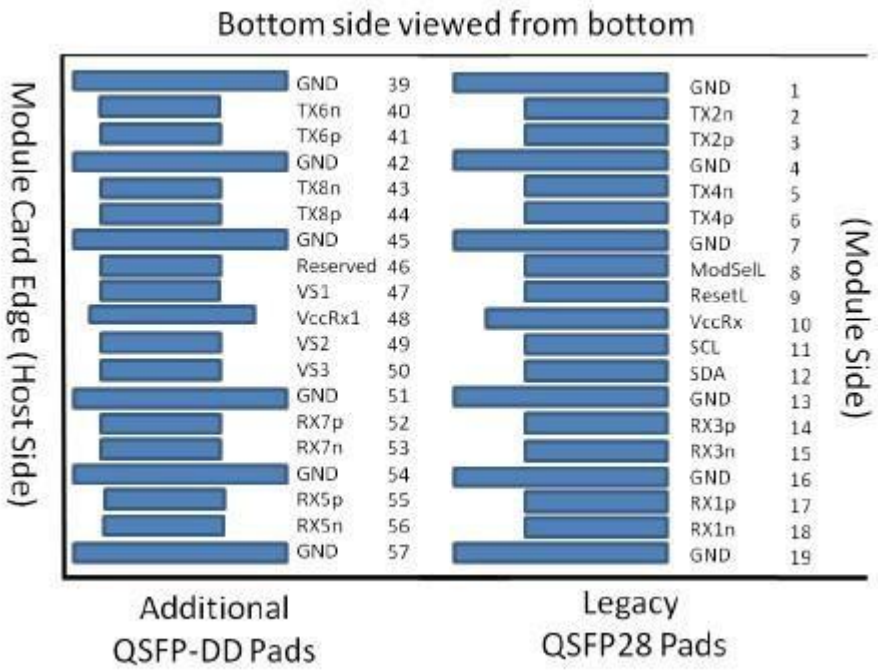


Figure 6 Module pad layout

Table 5: Pad Function Definition

Pad	Logic	Symbol	Description	Notes
1		GND	Ground	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	
4		GND	Ground	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	
7		GND	Ground	1
8	LVTTL-I	ModSelL	Module Select	
9	LVTTL-I	ResetL	Module Reset	
10		VccRx	+3.3V Power Supply Receiver	2
11	LVCMOS-I/O	SCL	2-wire serial interface clock	
12	LVCMOS-I/O	SDA	2-wire serial interface data	
13		GND	Ground	1
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	

15	CML-O	Rx3n	Receiver Inverted Data Output	
16		GND	Ground	1
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	
18	CML-O	Rx1n	Receiver Inverted Data Output	
19		GND	Ground	1
20		GND	Ground	1
21	CML-O	Rx2n	Receiver Inverted Data Output	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	
23		GND	Ground	1
24	CML-O	Rx4n	Receiver Inverted Data Output	
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	
26		GND	Ground	1
27	LVTTL-O	ModPrsL	Module Present	
28	LVTTL-O	IntL	Interrupt	
29		VccTx	+3.3V Power supply transmitter	2
30		Vcc1	+3.3V Power supply	2
31	LVTTL-I	InitMode	Initialization mode; In legacy QSFP applications, the InitMode pad is called LPMODE	
32		GND	Ground	1
33	CML-I	Tx3p	Transmitter Non-Inverted Data Output	
34	CML-I	Tx3n	Transmitter Inverted Data Output	
35		GND	Ground	1
36	CML-I	Tx1p	Transmitter Non-Inverted Data Output	
37	CML-I	Tx1n	Transmitter Inverted Data Output	
38		GND	Ground	1
39		GND	Ground	1
40	CML-I	Tx6n	Transmitter Inverted Data Output	
41	CML-I	Tx6p	Transmitter Non-Inverted Data Output	
42		GND	Ground	1
43	CML-I	Tx8n	Transmitter Inverted Data Output	

44	CML-I	Tx8p	Transmitter Non-Inverted Data Output	
45		GND	Ground	1
46		Reserved	For future use	3
47		VS1	Module Vendor Specific 1	3
48		VccRx1	3.3V Power Supply	2
49		VS2	Module Vendor Specific 2	3
50		VS3	Module Vendor Specific 3	3
51		GND	Ground	1
52	CML-O	Rx7p	Receiver Non-Inverted Data Output	
53	CML-O	Rx7n	Receiver Inverted Data Output	
54		GND	Ground	1
55	CML-O	Rx5p	Receiver Non-Inverted Data Output	
56	CML-O	Rx5n	Receiver Inverted Data Output	
57		GND	Ground	1
58		GND	Ground	1
59	CML-O	Rx6n	Receiver Inverted Data Output	
60	CML-O	Rx6p	Receiver Non-Inverted Data Output	
61		GND	Ground	1
62	CML-O	Rx8n	Receiver Inverted Data Output	
63	CML-O	Rx8p	Receiver Non-Inverted Data Output	
64		GND	Ground	1
65		NC	No Connect	3
66		Reserved	For future use	3
67		VccTx1	3.3V Power Supply	2
68		Vcc2	3.3V Power Supply	2
69		ePPS	Precision Time Protocol (PTP) reference clock input. It is not used	3
70		GND	Ground	1
71	CML-I	Tx7p	Transmitter Non-Inverted Data Input	
72	CML-I	Tx7n	Transmitter Inverted Data Input	

73		GND	Ground	1
74	CML-I	Tx5p	Transmitter Non-Inverted Data Input	
75	CML-I	Tx5n	Transmitter Inverted Data Input	
76		GND	Ground	1

Notes:

1. QSFP-DD uses common ground (GND) for all signals and supply (power). All are comon within the QSFP-DD module and all module voltages are referenced to this po-te-nial unless otherwise noted. Connect these directly to the host board signal-common ground plane.
2. VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 shall be applied concurrently.Requirements defined for the host side of the Host Card Edge Connector. VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 may be internally connected within the module in any combination. The connector Vcc pins are each rated for a maximum current of 1000 mA.
3. All Vendor Specific, Reserved and No Connect pins may be terminated with 50ohms to ground on the host. Pad 65 (No Connect) shall be left unconnected within the module. Vendor specific and Reserved pads shall have an impedance to GND that is greater than 10K ohms and less than 100pF.

3.3 Low Speed Control and Sense Signals

Table 6: Low Speed Control and Sense Signals

Parameter	Symbol	Min	Max	Unit	Condition
SCL and SDA	VOL	0	0.4	V	IOL(max)=3mA for fast mode, 20ma for Fast-mode plus
	VOH	Vcc-0.5	Vcc+0.3	V	
SCL and SDA	VIL	-0.3	Vcc*0.3	V	
	VIH	VCC*0.7	Vcc+0.5	V	
Capacitance for SCL and SDA I/O signal	Ci		14	pF	
Total bus capacitive load for SCL and SDA	Cb		100	pF	For 400kHz clock rate use 3.0 k Ohms Pullup resistor, max. For 1000kHz clock rate refer to Figure 40
			200	pF	For 400kHz clock rate use 1.6 k Ohms pullup resistor, max. For 1000kHz clock rate refer to Figure 40
	VIL	-0.3	0.8	V	

InitMode, ResetL and ModSelL	VIH	2	VCC+0.3	V	
	|Iin|		360	uA	0V<Vin<Vcc
IntL	VOL	0	0.4	V	IOL=2.0mA
	VOH	VCC-0.5	VCC+0.3	V	10k ohms pull up to Host Vcc
ModPrsL	VOL	0	0.4	V	IOL=2.0mA
	VOH				ModPrsL can be implemented as a short-circuit to GND on the module

3.4 I2C Timing Diagram

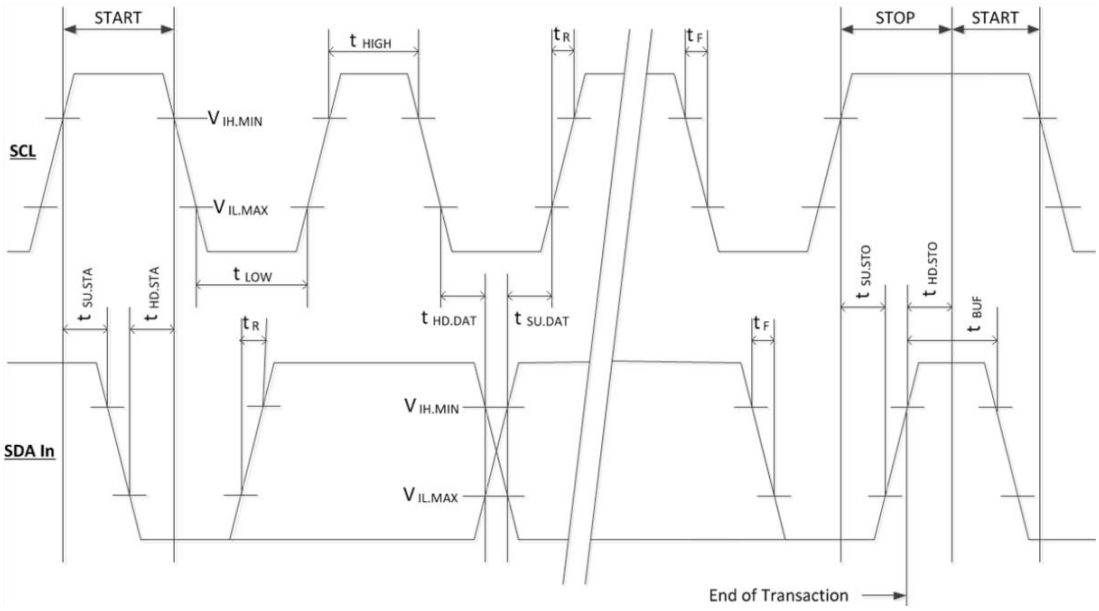


Figure 7 I2C Timing Diagram

		Fast Mode (400 KHz)		Fast Mode Plus(1 MHz)			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Conditions**

Clock Frequency	fSCL	0	400	0	1000	KHz	
Clock Pulse Width Low	tLOW	1.3		0.5		µs	
Clock Pulse Width Hig	tHIGH	0.6		0.26		µs	
Time bus free before new transmission can start	tBUF	20		1		µs	Between STOP and START and between ACK and ReStart

Table 7: Management Interface timing parameters

START Hold Time	tHD.STA	0.6		0.26		µs	The delay required between SDA becoming low and SCL starting to go low in a START
START Setup Time	tSU.STA	0.6		0.26		µs	The delay required between SCL becoming high and SDA starting to go low in a START
Data In Hold Time	tHD.DAT	0		0		µs	
Data In Setup Time	tSU.DAT	0.1		0.1		µs	
Input Rise Time	tR		300		120	ns	From (VIL,MAX=0.3*Vcc) to (VIH, MIN=0.7*Vcc)
Input Fall Time	tF		300		120	ns	From (VIH,MIN=0.7*Vcc) to (VIL,MAX=0.3*Vcc)
STOP Setup Time	tSU.STO	0.6		0.6		us	
STOP Hold Time	tHD.STO	0.6		0.26		us	

Aborted sequence -bus release	Deselect_Abort	2		2		ms	Delay from a host de-asserting ModSelL (at any point in a bus sequence) to the QSFP-DD module releasing SCL and SDA
ModSelL Setup Time1	tSU.ModSelL	2		2		ms	ModSelL Setup Time is the setup time on the select lines before the start of a host initiated serial bus sequence.
ModSelL Hold Time1	tHD.ModSelL	2		2		ms	ModSelL Hold Time is the delay from completion of a serial bus sequence to changes of module Select status.
Serial Interface Clock Holdoff “Clock Stretching”	T_clock_hold		500		500	us	Maximum time the QSFP-DD module may hold the SCL line low before continuing with a read or write operation
Complete Single	tWR		40		40	ms	Complete (up to) 4 Byte Write
Sequential Write							
Endurance (Write Cycles)		50K			50K	cycles	Module Case Temperature = 700C
Note 1: When the host has determined that module is QSFP-DD, the management registers can be read to determine alternate supported ModSelL set up and hold times.							

SDA/SCL options for pull-up resistor, bus capacitance and rise/fall times

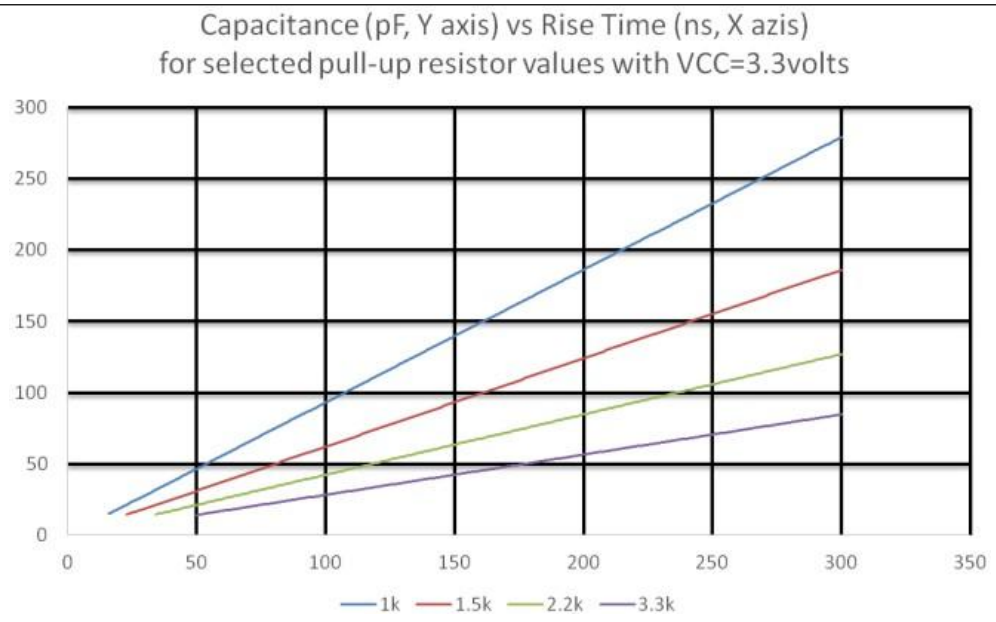


Figure 8 SDA/SCL options for pull-up resistor, bus capacitance and rise/fall times

3.5 High-Speed Electrical Specifications

The transmitter and receiver comply with the CEI-56G-VSR-PAM4 electrical specification. The data lines are AC-coupled and terminated in the module per the following figure from the QSFP-DD MSA.

Parameter	Symbol	Min	Typ	Max	Unit	Note
400GAUI-8 Electrical Characteristics						
Transmitter						
Signaling Rate, each lane			26.5625		GBd	PAM4
Differential Voltage pk-pk	Vin, pp			880	mV	
Common Mode Voltage	Vcm	-0.3		2.8	V	
Common Mode Noise	RMS			17.5	mV	
Differential Termination Resistance Mismatch				10	%	

Notes
1. 400GAUI-8 Electrical Characteristics refers to CEI-56G-VSR-PAM4 of OIF-CEI-04.0

Transition time	Trise/Tfall	12			ps	20%~80%
Eye Width at 10^{-6} probability	EW6	0.2			UI	
Eye Height at at 10^{-6} probability	EH6	32			mV	
Eye Linearity		0.85				
Receiver						
Signaling Rate, each lane			26.5625		GBd	PAM4
Differential Voltage pk-pk	Vout, pp			900	mV	

Transition time	Trise/Tfall	9.5			ps	20%~80%
Near-end eye width at 10^{-6} probability	EW6	0.265			UI	
Near-end eye height at 10^{-6} probability	EH6	70			mV	
Far-end eye width at 10^{-6} probability	EW6	0.2			UI	
Far-end eye height at 10^{-6} probability	EH6	30			mV	
Near-end Eye Linearity		0.85				

4 Optical Specifications

Table 8: Optical channel specifications

Parameter	Default	Min	Max	Unit	Conditions/Comments
Channel frequency	193.7	191.3	196.1	THz	ITU-T grid
Channel spacing†	100	100		GHz	Per ITU-T G694.1 Section 6.
	75	75		GHz	Per ITU-T G694.1 Section 6.
Fiber type	G.652				Single mode fiber. Specified for link budgeting purposes only.
Target reach		80	-	km	Amplified Link – Noise limited

†For channel spacing of 100 GHz on a fiber, the allowed channel frequencies (in THz) are defined by 193.1 + n × 0.1 where n is a positive or negative integer including 0. For 400ZR modules, n = 30 to -17 in steps of 1. The specified 48 × 100GHz DWDM application channels are as defined below.

Index	n(from ITU-T G.694.1)	Freq.(THz)
1	30	196.100
2	29	196.000
3	28	195.900
…	…	…
46	-15	191.600
47	-16	191.500
48	-17	191.400

†For channel spacing of 75 GHz or more on a fiber, the allowed channel frequencies (in THz) are defined by 193.1 + 3n × 0.025 where n is a positive or negative integer including 0. For 400ZR modules, 3n = 120 to -69. The reference 64 × 75 GHz DWDM application channels are as defined below.

Index	n(from ITU-T G.694.1)	Freq.(THz)
1	120	196.100
2	117	196.025

3	114	195.950
…	…	…
62	-63	191.525
63	-66	191.450
64	-69	191.375

Table 9: Transmitter Optical Specifications

Parameter	Typ	Min	Max	Unit	Condition/comments
Transmitter frequency range		191.3	196.1	THz	ITU-T grid. Frequency range over which the specifications hold unless noted otherwise
Transmitter laser frequency stability		-1.8	1.8	GHz	Offset from channel frequency set point. The receiver LO has the same frequency accuracy.
Transmitter output power		-10	-6	dBm	Measured at optical connector.
Transmitter Output power with TX disabled			-20	dBm	Max Output power with TX_DIS asserted
Transmitter Output power during wavelength switching			-20	dBm	
Transmitter reflectance			-20	dB	Loss of power in the returned/reflected optical signal
Mean I-Q amplitude imbalance			1	dB	
Transmitter polarization dependent power			1.5	dB	Power difference between X and Y polarization

Table 10: Receiver Optical Specification

Parameter	Min	Max	Unit	Conditions/Comments
Frequency offset between RX and LO	-3.6	3.6	GHz	Acquisition Range

Input power range	-12	0	dBm	
Input sensitivity	-12		dBm	
OSNR Tolerance		26	dB/0.1nm	The OSNR tolerance is referenced to an optical bandwidth of 0.1nm @193.7 THz or 12.5 GHz.
Optical return loss	20		dB	Optical reflectance at connector input
CD Tolerance	2400		ps/nm	Tolerance to Chromatic Dispersion
Optical path power penalty		0.5	dB	OSNR penalty tolerance due to -35dB interferometric crosstalk and 2400ps/nm chromatic dispersion.
PMD tolerance	10	-	ps	Tolerance to PMD with ≤0.5 dB penalty to OSNR sensitivity.10ps of PMD corresponds to max 30 ps of DGD and max 500 ps2 of SOPMD
PDL tolerance	3.5	-	dB	Tolerance to PDL with <1.3 dB penalty to OSNR sensitivity When change in PSP is < =1 rad/ms

Tolerance to change in SOP	50	-	rad/ms	Tolerance to change in SOP with ≤0.5dB penalty to OSNR sensitivity, Measurement relative to reference with 10 ps PMD and 2.5 dB PDL and SOP of < 1 rad/ms under the same conditions.
Optical input power transient tolerance	+/-2	-	dB	Tolerance to change in input power with ≤ 0.5dB penalty to OSNR sensitivity.Received power is within-12~0dBm,Rise/fall times of power change defined by 20-80% of 50us or slower.

Table 11: TX Specification

Parameter	Min	Max	Unit	Conditions/Comments
Transmitter laser disable time		100	ms	The maximum transmitter turn-off time from any condition that results in Tx_Disable==true to reach the Tx output power -20dBm. Rx shall remain locked and thus LO must remain enabled.
Transmitter turn-up time from warm start		180	Sec	he maximum time from ModuleLowPwr to DataPathActivated state.
Transmitter turn-up time from cold start		200	Sec	The maximum time from deassertion of ResetS == false to DataPathActivated state while LoPwrS == false.
Transmitter wavelength switching time		180	Sec	The maximum time to change wavelengths including turn-up time.
Output power monitor - Accuracy	-2	2	dB	Total output power measurement including all ASE contribution. Measurement accuracy does not contribute to Allowable output power signal window

Table 12: RX Specification

Parameter	Default	Min	Max	Unit	Conditions/Comments
Receiver turn-up time from warm start			10	Sec.	Upon Rx_LOS de-assert, Receiver has been turned up previously.
Receiver turn-up time from cold start			200	Sec.	From module reset, with valid optical input signal present.
Input total power monitor - Accuracy		-4	4	dB	Over the combined range of receiver sensitivity input power ranges and the optical LOS Assert threshold range.
Input Channel power monitor - Accuracy		-4	4	dB	The module reports the channel power as received by the module.
Optical LOS Assert Threshold	-18	-20	-16	dBm	Channel Power
Optical LOS Hysteresis		1	2.5	dBm	RX LOS cleared

5 Typical Application Circuits

The typical application circuits for our QSFP-DD-400G-ZR optical module interface, special I/O pins and the power supply decoupling are shown as below.

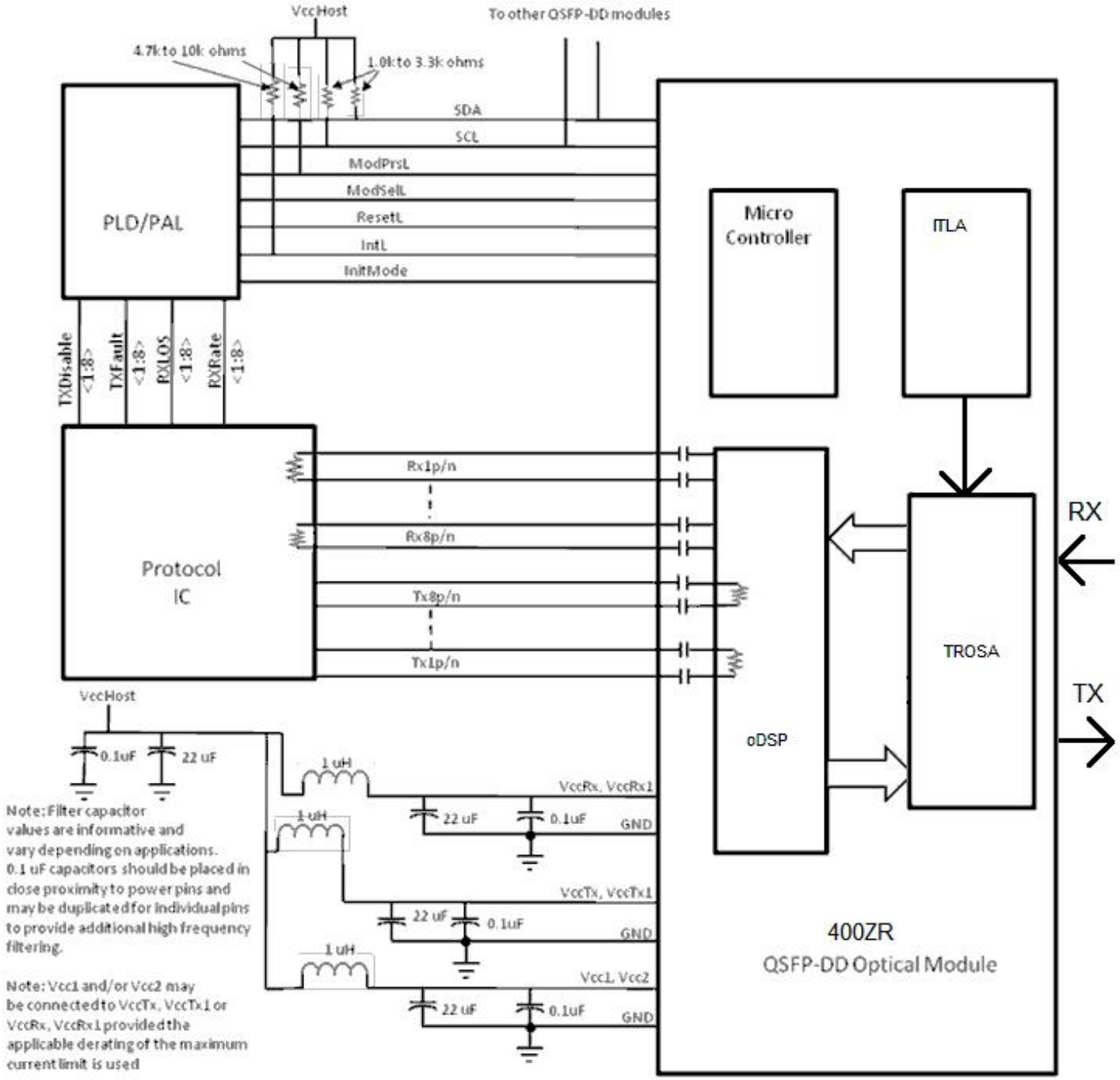


Figure 9 Example QSFP-DD Host Board Schematic for 400ZR Optical Modules

6.1 Mechanical Dimensions

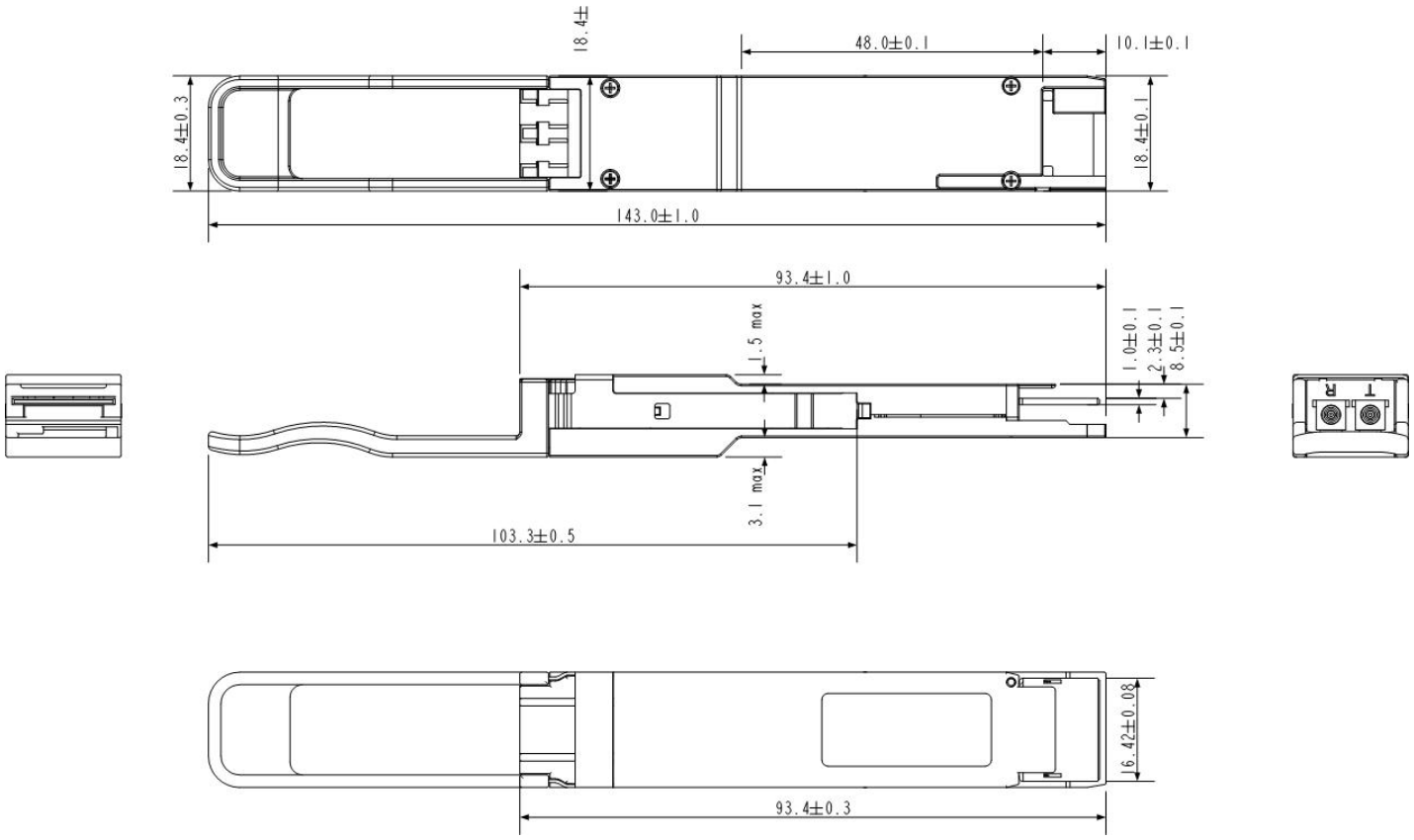


Figure 10 Mechanical Dimensions

6.2 Dual LC Optical Cable connection

The Dual LC optical patchcord and module receptacle is specified in TIA-604-10 and shown below

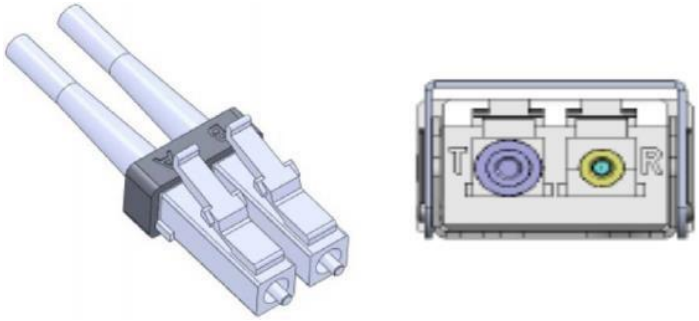


Figure 11 optical interface

7 Memory Contents

The QSFP-DD-400G-ZR transceivers conform to QSFP-DD MSA Management Interface Specifications, Rev 4.0, also conform to coherent CMIS MSA OIF-C-CMIS-01.0, and support the online software update feature which is defined in QSFP-DD MSA Management Interface Specifications.

8 Regulatory and Reliability Specifications

8.1 Laser Safety

The module is designed to comply with Class 1 laser, according to IEC/EN 60825-1/A2: 2001, or FDA CDRH21 CFR-1040. Don't directly look into the transmitter fiber connector at any time while the module is in operation.

8.2 ESD

The module is subjected to 15kV air discharges during operation and 8kV direct contact discharges to the case. All the pins including high speed signal pins can withstand 1000 V electrostatic discharge based on Human Body Model per ANSI/ESDA/JEDEC JS-001.

8.3 Electromagnetic Emission

The module is designed to comply with Class B electromagnetic emission according to GR-1089-CORE Sections.

3.2.1.1 and 3.2.1.3

8.4 Electromagnetic Immunity

The module is designed to comply with EMI 8.5V/m per GR.1089-CORE section 3.3.1.

8.5 Flammability

The module is designed to comply with GR-63 section 4.2.3 for fire resistance.

8.6 RoHS

The module complies with Directive 2002/95/EC on the restriction on the use of certain hazardous substances in electrical and electronic equipment and with exception 6a, 6c, 7b and 13a permitted by Commission Decision (2010/571/EU).

8.7 Reliability

The module is designed to comply with GR-468 for general reliability. Target FIT <1000 at 50℃ operating case temperature.

9 References

1. OIF-400ZR-01.0: Implementation Agreement 400ZR
2. QSFP-DD-Hardware-rev5.1: QSFP-DD Hardware Specification
3. OIF-C-CMIS-01.0: Implementation Agreement for Coherent CMIS
4. OIF-CEI-56G-VSR-PAM4 Very Short Reach Interface (OIF-CEI-04.0), 56 Gb/s chip-to-module PAM4 electrical interface for use in the range 18.0 to 29.0 Gsym/s with up to 10.0 dB loss at the Nyquist frequency, including one connector
5. IEEE Std 802.3™-2018 (Revision of IEEE Std 802.3-2015)
6. G694.1: Spectral grids for WDM applications: DWDM Frequency grid.
7. Telcordia NEBS™ Requirements: Physical Protection, Telcordia Technologies Generic Requirements, GR-63-CORE Issue 3, March 2006.
8. GR-468-CORE General Reliability Assurance Requirements for Optoelectronic Devices used in Telecommunications Equipment.