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RELATED DOCUMENTS

Doc. Number	Doc. Title
1	CFP MSA CFP2 Hardware Specification, Revision 1.0 31 July 2013
2	OIF-CFP2-DCO-01.0 – Implementation Agreement for Digital Coherent Optics Module (October 2018)
3	CFP2 MSA Management Interface – 100/40 Gigabit Transceiver Package Multi-Source Agreement, Version 2.6 r06a, March 24th, 2017
4	IEEE Standard for Local and metropolitan area networks—Station and Media Access Control Connectivity Discovery, 802.1AB, 2016
5	ITU-T G.709/Y.1331
6	ITU-T G.7712
7	ITU-T G.798
8	IEEE 802.3-2018
9	ISO9001 Quality management systems — Requirements

1 SCOPE

The document outlines the product specifications of 400G Digital Coherent Optics with CFP2 form factor (CFP2DCO) Transceiver. The specification includes absolute maximum rating, optical specification, electrical/mechanical specification, optical performance criteria, fault management, performance monitoring, and other common product requirement.

2 PRODUCT DESCRIPTION

The CFP2 DCO supports multi-rate coherent transmission for data centre interconnect, metro, and long-haul transport applications. It is an OpenZR+/FlexO compliant module. On the client side, the module can accommodate a variety of signal types including 100GBE, 200GBE, 400GBE. On the line side, the module supports 200G and 400G interfaces with different modulation formats and forward error correction (FEC) code. Multiple 100G clients or 200G clients can be multiplexed onto a single 200G or 400G line side interface.

The transceiver module is compliant to the CFP MSA CFP2 Hardware Specification [1], with extensions specified in the OIF CFP2-DCO implementation agreement [2]. The transceiver is RoHS compliant and lead-free per Directive 2011/65/EU.

This specification is defined for CFP2 DCO using Acacia Greylock DSP version 1.0 (GL1).

Greylock DSP version 2.0 (GL2) information is provided but will be elaborated after GA.

3 GENERAL SPECIFICATION

All values specified in the document indicate worst-case End of Life (EOL) specifications unless otherwise stated.

3.1 General Product Description

Table 1 shows the general description of each device and its associated customer part number. All wavelengths refer to wavelengths in vacuum. Refer to OIF standard for contents not mentioned in this specification.

Table 1: General Product Description

NO.	Manufacturing PN	Description	Description in EDT	Note
1	OPC2J-DCO-GL1	400G CFP2DCO Transceiver	400G_CFP2_DCO	GL1
2	OPC2J-DCO-GL2			GL2

Features only applied in GL2 version will be explicitly highlighted with characters "**[GL2]**".

3.2 Absolute Maximum Ratings

Ratings illustrated in Table 2 refer to conditions applied to the device under which the device will not be damaged and must be fully recovered to its specified performance. Unless otherwise stated, typical test environment is e.g., in normal laboratory or manufacturing area under ambient condition.

Table 2: Absolute Maximum Ratings

Parameters	Symbol	Min.	Typ.	Max.	Unit
Operating Case Temperature		-5		80	℃

DC Supply Voltage	Vcc	3.135	3.3	3.465	V
Receiver Maximum Input Power (Single channel)				13	dBm
Receiver Maximum Input Power (WDM channel)				15	dBm

3.3 Operating Environment and Requirements

The operating environment is the set of operating conditions in which the device is expected to operate and meet the optical performance as specified in Table 3. The normal operating condition environment is defined as all possible combinations of the following conditions.

Table 3: Operating Environment

Parameter	Conditions	Min	Typ	Max	Unit
Environmental Storage Temperature		-40		+85	℃
Environmental Case Operating Temperature	Long-term	0		70	℃
	Short-term: the module operates up to a maximum temperature for short term (96 Hours continuously, no more than 15 days per year)			80	℃
Environmental Operating Relative Humidity	Non-condensing	5		85	%
Environmental Storage Relative Humidity		5		85	%

3.4 Modes of Operation

3.4.1 Network Lane Interface

Table 4: Modes of Operation Supported

Category	FEC	OH	Framing Format	Baudrate (GBd)	Bitrate (Gbit/s)	Max Power（W）
OpenZR+	oFEC	15%	200G-200ZR-OFEC-QPSK	60.1385468	240.550	24.0
			400G-400ZR-OFEC-16QAM		481.110	26.0
FlexO Streaming			200G-FOIC2-OFEC-QPSK **[GL2]**	63.139467923	253.250	24.0
			400G-FOIC4-OFEC-16QAM **[GL2]**		506.500	26.0

3.4.2 Network Lane Interface FEC Capability

Table 5: FEC Capability

FEC	OH	Net Coding Gain (dB)	FEC Limit

oFEC	15%	11.6	2.0e-2

3.4.3 Network Lane Interface to Client Interface Mapping

Table 6: Network to Client Interface Mapping

Framing Format	Client Interface #	Client Interface Type	MDI Interface	Baudrate (GBd)	Modulation	FEC	Skew Tolerance
200G-200ZR-OFEC-QPSK 200G-FOIC2-OFEC-QPSK **[GL2]**	2	100GBASE-R	CAUI-4	25.781250	NRZ	RS-FEC (528,514) *	180 ns
			100GAUI-2	26.562500	PAM4	RS-FEC (544,514)	
	1	200GBASE-R	200GAUI-4	26.562500	PAM4	RS-FEC (544,514)	
400G-400ZR-OFEC-16QAM 400G-FOIC4-OFEC-16QAM **[GL2]**	4	100GBASE-R	100GAUI-2	26.562500	PAM4	RS-FEC (544,514)	
	2	200GBASE-R	200GAUI-4	26.562500	PAM4	RS-FEC (544,514)	
	1	400GBASE-R	400GAUI-8	26.562500	PAM4	RS-FEC (544,514)	

*: indicates the FEC can be switched off.

Table 7: Client Interface to DCO Client SerDes Lane Mapping

SerDes Lanes	400G	200G [GL2]	100G	
	400GAUI-8 OTUC4 [GL2] FOIC4.8 [GL2] (PAM4)	200GAUI-4 [GL2] OTUC2 [GL2] FOIC2.4 [GL2] (PAM4)	CAUI-4 OTLC.4 [GL2] OTL4.4 [GL2] (NRZ)	100GAUI-2 OTLC.2 [GL2] OTL4.2 [GL2] (PAM4)
	Interface - CH[x,y]			
Tx7[p,n];Rx7[p,n]	CH4.1	CH2.2	CH1.2	CH1.4
Tx6[p,n];Rx6[p,n]				
Tx5[p,n];Rx5[p,n]				CH1.3
Tx4[p,n];Rx4[p,n]				
Tx3[p,n];Rx3[p,n]		CH2.1	CH1.1	CH1.2
Tx2[p,n];Rx2[p,n]				
Tx1[p,n];Rx1[p,n]				CH1.1
Tx0[p,n];Rx0[p,n]				

The CFP2 Host/Client interface naming convention is **CH<x>.<y>** where,

- CH=Channel,
- **<x>** = channel capacity, where [x=1,2,4] is 1=100G, 2=200G, or 4=400G,
- **<y>** = channel enumeration, where [y= 1…4] is the channel enumeration

3.5 Optical Characteristics

Note: All specifications are within all above operating environment defined in Table 3.

3.5.1 Transmitter Optical Characteristics

Table 8: Transmitter Optical Characteristics

Parameter	Measurement Conditions	Min	Typ	Max	Unit	Comments
Tx output power	DP-QPSK	-7		0	dBm	Tx VOA set to minimum.
	DP-16QAM					Regardless framing format
Shuttered output power				-35	dBm	
Tx output power during wavelength switch				-40	dBm	
Wavelength range		1528.77		1567.14	nm	
Frequency range		191.3		196.1	THz	
Channel grid spacing	Across C-band	6.25	75	100	GHz	
Frequency bright tuning	Fine tuning with Tx output enabled	-6.25		6.25	GHz	Acacia complies to +/6 GHz
Fine detuning resolution		0.1			GHz	
Laser linewidth	Tx and LO			300	kHz	
Frequency accuracy		-1.5		1.5	GHz	
Laser RIN at max output power	avg			-145	dB/Hz	0.2≤f≤10 (GHz)
	peak			-140		
Tx in-band OSNR		45			dB	Acacia complies to 40 dB
Tx out-of-band OSNR		40			dB	No TOF version, Acacia complies to 29
Tx VOA tuning range				11	dB	
Tx output power stability	Tx VOA = 0	-0.5		+0.5	dB	
	Tx VOA > 0	-1		+1	dB	
Optical Tx turn on time	Warm start			1	s	Acacia complies to 5 s due to EDFA bring-up
	Cold start			60	s	Acacia complies to 121 s due to EDFA bring-up
Optical Tx turn off time	From Tx_DIS activated			10	ms	Laser turned off time
Tx Ch-to-Ch switching time	Beyond ±6.25GHz			60	s	Acacia complies to 91s w/ modulator bias optimization
	Within ±6.25GHz				s	Acacia complies to 200s w/ modulator bias optimization

Tx optical return loss	Towards the module	27			dB	Ratio of the power reflected by the device to the power incident on the device.

3.5.2 Receiver Optical Characteristics

Table 9: Receiver Optical Characteristics

Parameter	Measurement Conditions	Min	Typ	Max	Unit	Comments
Rx Sensitivity	200G-200ZR-OFEC-QPSK	-22			dBm	Full OSNR Tx<->Rx b2b
	400G-400ZR-OFEC-16QAM	-18				
	200G-FOIC2-OFEC-QPSK **[GL2]**	-22				
	400G-FOIC4-OFEC-16QAM **[GL2]**	-18				
Rx reflectance				-20	dB	Pref/Pin [dB]
LO to Rx leakage				-32	dBm	
Rx LO to Tx carrier offset		-3.6		3.6	GHz	Acquisition range
Rx turn up time	Warm start			30	ms	Rx_LOS de-assert
	Cold start			120	s	Module reset w/ Sig present
Rx CD Setting Range	200G-200ZR-OFEC-QPSK	-50		50	ns/nm	
	400G-400ZR-OFEC-16QAM	-26		26		
	200G-FOIC2-OFEC-QPSK **[GL2]**	-48		48		
	400G-FOIC4-OFEC-16QAM **[GL2]**	-24		24		
Rx acquisition time			30	50	ms	Max CD search range á la modes
Rx VOA range		10			dB	
Rx VOA step size				0.4	dB	
Rx VOA response time				100	ms	
Rx LOS Threshold	200G-200ZR-OFEC-QPSK	-35			dBm	DSP should be first LOL then LOS.
	400G-400ZR-OFEC-16QAM	-28				
	200G-FOIC2-OFEC-QPSK **[GL2]**	-35				
	400G-FOIC4-OFEC-16QAM **[GL2]**	-27.5				
Rx LOS Hysteresis		0.3		2.5	dB	

Table 10: Optical Parameter Monitoring Accuracy

Item	Min	Max	Unit	Condition
Dispersion reading	Min{-100, 3%*D_{est}}	Max{+100, 3%*D_{est}}	%	Reports the actual link CD
DGD reading	-10	+10	ps	Reports the actual link DGD
PDL reading	-1.5	+1.5	dB	Only for less than 3dB PDL range
Input total power reading	-1.5	+1.5	dB	Between -25 to +4dBm
	-2.5	+2.5		Between -33 to +4dBm
Input signal OSNR reading	-1.5	1.5	dB	For OSNR 5dB above corresponding required OSNR listed in Table 11 with Pin > -12 dBm

3.6 Rx Performance Specification

3.6.1 Required OSNR w/ ASE Noise

Table 11: Required OSNR Baseline EOL

Parameter	Measurement Conditions	Min	Typ	Max	Unit	Comments
Required OSNR	200G-200ZR-OFEC-QPSK		14	14.5	dB	Comply
	400G-400ZR-OFEC-16QAM		21.5	22.5		Comply
	200G-FOIC2-OFEC-QPSK **[GL2]**		14	14.5		Acacia offers max 15.7 dB
	400G-FOIC4-OFEC-16QAM **[GL2]**		21.5	22.5		Acacia offers max 24 dB

3.6.2 Rx Power Variation

Table 12: OSNR Penalty due to Rx Power Variation

Parameter	Mode	0 dB OSNR penalty	0.5 dB OSNR penalty	Unit
Rx dynamic range	200G-200ZR-OFEC-QPSK	-18	-20	dBm
	400G-400ZR-OFEC-16QAM	-12	-14	
	200G-FOIC2-OFEC-QPSK **[GL2]**	-18	-20	
	400G-FOIC4-OFEC-16QAM **[GL2]**	-10	-14	

3.6.3 Filtering Penalty

Signal Spectrum has roll-off factor of 0.2. Filter is placed before noise loading after Tx.

Table 13: OSNR Penalty due to Filtering Penalty

Parameter	Mode	B_{3dB} causes 0.5 dB OSNR penalty	Filter Type
Filtering	200G-200ZR-OFEC-QPSK	66 GHz	2nd Order Super Gaussian

OSNR Penalty	400G-400ZR-OFEC-16QAM	74 GHz	
	200G-FOIC2-OFEC-QPSK **[GL2]**	68 GHz	
	400G-FOIC4-OFEC-16QAM **[GL2]**	77 GHz	

3.6.4 CD Tolerance

Table 14: OSNR Penalty due to CD

Parameter	Mode	0.5 dB OSNR Penalty	Unit
CD Tolerance	200G-200ZR-OFEC-QPSK	40,000	ps/nm
	400G-400ZR-OFEC-16QAM	20,000	
	200G-FOIC2-OFEC-QPSK **[GL2]**	40,000	
	400G-FOIC4-OFEC-16QAM **[GL2]**	20,000	

3.6.5 PMD Tolerance

Table 15: OSNR Penalty due to PMD

Parameter	Mode	0.5 dB OSNR Penalty
PMD Tolerance	200G-200ZR-OFEC-QPSK	DGD 42 ps, SOPMD 900 ps^2
	400G-400ZR-OFEC-16QAM	
	200G-FOIC2-OFEC-QPSK **[GL2]**	
	400G-FOIC4-OFEC-16QAM **[GL2]**	

3.6.6 SOP Tolerance

Table 16: OSNR Penalty due to SOP Rotation

Parameter	Mode	0.5 dB OSNR Penalty	Unit
SOP Tolerance	200G-200ZR-OFEC-QPSK	400	krad/s
	400G-400ZR-OFEC-16QAM	50	
	200G-FOIC2-OFEC-QPSK **[GL2]**	400	
	400G-FOIC4-OFEC-16QAM **[GL2]**	50	

*: with enhanced SOP tracking mode enabled.

3.7 Electrical Characteristics

Electrical performance shall strictly follow standard: IEEE Std 802.3-2018 and OIF-CFP2-DCO-01.0.

3.7.1 PIN Definition

The detail PIN definition is listed in Table 17.

Table 17: PIN Definition (Bottom)

PIN Number	Name of Pin	Structure (Input / Output)	Logic	Description / Connection
1	GND	GND	Ground	
2	OHIO_RDn (TX_MCLKn)	O	CML	OHIO Drop interface; Interface is differentially AC coupled, internal to module.
3	OHIO_RDp (TX_MCLKp)	O	CML	
4	GND	GND	Ground	
5	OHIO_TDn (N.C.)	I	CML	OHIO Insert interface; Interface is differentially AC coupled, terminated, and biased internal to module.
6	OHIO_TDp (N.C.)	I	CML	
7	3.3V GND	PWR_GND	Ground	3.3V Module Supply Voltage Return Ground, can be separate or tied together with Signal Ground
8	3.3V GND	PWR_GND	Ground	3.3V Module Supply Voltage Return Ground, can be separate or tied together with Signal Ground
9	3.3V	PWR	Power	3.3V Module Supply Voltage
10	3.3V	PWR	Power	3.3V Module Supply Voltage
11	3.3V	PWR	Power	3.3V Module Supply Voltage
12	3.3V	PWR	Power	3.3V Module Supply Voltage
13	3.3V GND	PWR_GND	Ground	3.3V Module Supply Voltage Return Ground, can be separate or tied together with Signal Ground
14	3.3V GND	PWR_GND	Ground	3.3V Module Supply Voltage Return Ground, can be separate or tied together with Signal Ground
15	VND_IO_A	I/O	N.C	Module Vendor I/O A. Do Not Connect!
16	VND_IO_B	I/O	N.C	Module Vendor I/O B. Do Not Connect!
17	PRG_CNTL1	I	LVCMOS w/PUR	Programmable Control 1 set over MDIO; MSA Default: TRXIC_RSTn, TX & RX ICs reset, "0": reset, "1" or NC: enabled = not used
18	PRG_CNTL2	I	LVCMOS w/PUR	Programmable Control 2 set over MDIO; MSA Default: Hardware Interlock LSB, "00": ≤ 9W, "01": ≤12W, "10": ≤15W, "11" or NC: ≤ 18W = not used
19	PRG_CNTL3	I	LVCMOS w/PUR	Programmable Control 3 set over MDIO; MSA Default: Hardware Interlock MSB, "00": ≤ 9W, "01": ≤12W, "10": ≤15W, "11" or NC: ≤ 18W = not used

20	PRG_ALRM1	O	LVCMOS	Programmable Alarm 1; MSA Default “H” = HIPWR_ON
21	PRG_ALRM2	O	LVCMOS	Programmable Alarm 2; MSA Default “H” = MOD_READY
22	PRG_ALRM3	O	LVCMOS	Programmable Alarm 3; MSA Default “H” = MOD_FAULT
23	GND	GND	Ground	
24	TX_DIS	I	LVCMOS w/PUR	Transmitter Disable for all lanes, "1" or NC = transmitter disabled, "0" = transmitter enabled
25	RX_LOS	O	LVCMOS	Receiver Loss of Optical Signal, "1": low optical signal, "0": normal condition
26	MOD_LOPWR	I	LVCMOS w/PUR	Module Low Power Mode. "1" or NC: module in low power (safe) mode, "0": power-on enabled
27	MOD_ABS	O	GND	Module Absent;
28	MOD_RSTn	I	LVCMOS w/PUR	Module Reset. "0" resets the module, "1" or NC = module enabled, Pull Down Resistor in Module
29	GLB_ALRMn	O	LVCMOS	Global Alarm. “0": alarm condition in any MDIO Alarm register, "1": no alarm condition, Open Drain, Pull Up Resistor on Host
30	GND	GND	Ground	
31	MDC	I	1.2V LVCMOS	Management Data Clock (electrical specs as per IEEE Std 802.3- 2012)
32	MDIO	I/O	1.2V LVCMOS	Management Data I/O bi-directional data (electrical specs as per IEEE Std 802.3-2012)
33	PRTADR0	I	1.2V LVCMOS	MDIO Physical Port Address bit 0
34	PRTADR1	I	1.2V LVCMOS	MDIO Physical Port Address bit 1
35	PRTADR2	I	1.2V LVCMOS	MDIO Physical Port Address bit 2
36	VND_IO_C	I/O	N.C	Module Vendor I/O C. Do Not Connect!
37	MSA_BER_Threshold	O	3.3V LVCMOS	BER Threshold signal alarm;
38	VND_IO_E	I/O	N.C	Module Vendor I/O E. Do Not Connect!
39	3.3V GND	PWR_GND	Ground	Power Ground. Internally connected to logic GND. power supply return path.
40	3.3V GND	PWR_GND	Ground	Power Ground. Internally connected to logic GND. power supply return path.
41	3.3V	PWR	Power	3.3V power supply
42	3.3V	PWR	Power	3.3V power supply

43	3.3V	PWR	Power	3.3V power supply
44	3.3V	PWR	Power	3.3V power supply
45	3.3V GND	PWR_GND	Ground	Power Ground. Internally connected to logic GND. power supply return path.
46	3.3V GND	PWR_GND	Ground	Power Ground. Internally connected to logic GND. power supply return path.
47	OHIO_REFCLKn (N.C.)	I	CML	OHIO reference clock: Interface is AC coupled, biased, and terminated internal to module. If not using OHIO interface leave unconnected.
48	OHIO_REFCLKp (N.C.)	I	CML	
49	GND	GND	Ground	Module Ground. Logic and power return path
50	(RX_MCLKn) or Vendor_Out1n	O	CML	Not connected internally
51	(RX_MCLKp) or Vendor_Out1p	O	CML	
52	GND	GND	Ground	Module Ground. Logic and power return path

Table 18: PIN Definition (TOP)

PIN Number	Name						Description
	4x25G NRZ	8x25G NRZ	2x50G PAM4	4x50G PAM4	6x50G PAM4	8x50G PAM4	
104	GND	GND	GND	GND	GND	GND	Ground
103	N.C.	TX4n	N.C.	N.C.	TX4n	TX4n	Transmitter lane 4 / N.C
102	N.C.	TX4p	N.C.	N.C.	TX4p	TX4p	
101	GND	GND	GND	GND	GND	GND	Ground
100	TX3n	TX3n	N.C.	TX3n	TX3n	TX3n	Transmitter lane 3 / N.C
99	TX3p	TX3p	N.C.	TX3p	TX3p	TX3p	
98	GND	GND	GND	GND	GND	GND	Ground
97	TX2n	TX2n	N.C.	TX2n	TX2n	TX2n	Transmitter lane 2 / N.C
96	TX2p	TX2p	N.C.	TX2p	TX2p	TX2p	
95	GND	GND	GND	GND	GND	GND	Ground
94	N.C.	TX5n	N.C.	N.C.	TX5n	TX5n	Transmitter lane 5 / N.C
93	N.C.	TX5p	N.C.	N.C.	TX5p	TX5p	
92	GND	GND	GND	GND	GND	GND	Ground
91	N.C.	TX6n	N.C.	N.C.	N.C.	TX6n	Transmitter lane 6 / N.C
90	N.C.	TX6p	N.C.	N.C.	N.C.	TX6p	
89	GND	GND	GND	GND	GND	GND	Ground
88	TX1n	TX1n	TX1n	TX1n	TX1n	TX1n	Transmitter lane 1
87	TX1p	TX1p	TX1p	TX1p	TX1p	TX1p	
86	GND	GND	GND	GND	GND	GND	Ground

85	TX0n	TX0n	TX0n	TX0n	TX0n	TX0n	Transmitter lane 0
84	TX0p	TX0p	TX0p	TX0p	TX0p	TX0p	
83	GND	GND	GND	GND	GND	GND	Ground
82	N.C.	TX7n	N.C.	N.C.	N.C.	TX7n	Transmitter lane 7 / N.C
81	N.C.	TX7p	N.C.	N.C.	N.C.	TX7p	
80	GND	GND	GND	GND	GND	GND	Ground
79	*(REFCLKn)*	*(REFCLKn)*	*(REFCLKn)*	*(REFCLKn)*	*(REFCLKn)*	*(REFCLKn)*	N.C
78	*(REFCLKp)*	*(REFCLKp)*	*(REFCLKp)*	*(REFCLKp)*	*(REFCLKp)*	*(REFCLKp)*	
77	GND	GND	GND	GND	GND	GND	Ground
76	N.C.	RX4n	N.C.	N.C.	RX4n	RX4n	Receiver lane 4 / N.C
75	N.C.	RX4p	N.C.	N.C.	RX4p	RX4p	
74	GND	GND	GND	GND	GND	GND	Ground
73	RX3n	RX3n	N.C.	RX3n	RX3n	RX3n	Receiver lane 3 / N.C
72	RX3p	RX3p	N.C.	RX3p	RX3p	RX3p	
71	GND	GND	GND	GND	GND	GND	Ground
70	RX2n	RX2n	N.C.	RX2n	RX2n	RX2n	Receiver lane 2 / N.C
69	RX2p	RX2p	N.C.	RX2p	RX2p	RX2p	
68	GND	GND	GND	GND	GND	GND	Ground
67	N.C.	RX5n	N.C.	N.C.	RX5n	RX5n	Receiver lane 5 / N.C
66	N.C.	RX5p	N.C.	N.C.	RX5p	RX5p	
65	GND	GND	GND	GND	GND	GND	Ground
64	N.C.	RX6n	N.C.	N.C.	N.C.	RX6n	Receiver lane 6 / N.C
63	N.C.	RX6p	N.C.	N.C.	N.C.	RX6p	
62	GND	GND	GND	GND	GND	GND	Ground
61	RX1n	RX1n	RX1n	RX1n	RX1n	RX1n	Receiver lane 1
60	RX1p	RX1p	RX1p	RX1p	RX1p	RX1p	
59	GND	GND	GND	GND	GND	GND	Ground
58	RX0n	RX0n	RX0n	RX0n	RX0n	RX0n	Receiver lane 0
57	RX0p	RX0p	RX0p	RX0p	RX0p	RX0p	
56	GND	GND	GND	GND	GND	GND	Ground
55	N.C.	RX7n	N.C.	N.C.	N.C.	RX7n	Receiver lane 7
54	N.C.	RX7p	N.C.	N.C.	N.C.	RX7p	
53	GND	GND	GND	GND	GND	GND	Ground

3.8 Module Management Timing Characteristics

The module management interface shall fully comply to [3].

Table 19: Module Management Timing Characteristics

Parameter	Conditions	Min	Max	Unit	Note

MDC	Time interval between two consecutive rising or falling MDC edge	250		ns	
Host MDIO set-up time	Time interval for which Host MDIO signal must be stable prior to the sampling event of the MDC.	10		ns	
Host MDIO hold time	Time interval for which the Host MDIO signal must be stable following the sampling event of the MDC	10		ns	
MDC to CFP2 MDIO delay	Time delay among MDC falling edge and CFP2 MDIO state change	0	175	ns	
MOD_RSTn assert time	Between falling edge of MOD_RSTn and module entering Reset state		5	ms	
MOD_RSTn de-assert time	Between falling edge of MOD_RSTn and module entering Reset state		2.5	s	
MOD_LOPWR assert time	Between rising edge of MOD_LOPWR and module entering Low-Power state		1	ms	Acacia complies to 2 s
MOD_LOPWR de-assert time	Between falling edge of MOD_LOPWR and exit of the module from High-Power-up state		10	s	Acacia complies to 121 s
TX_DIS assert time	Between rising edge of TX_DIS and fall of lane output power below 10 % of nominal		1	ms	Acacia complies to 10 ms
TX_DIS de-assert time	Between falling edge of TX_DIS and rise of lane output power above 90 % of nominal		5	s	Module is in Ready state. The maximum transmitter turn-up time is counted from de-assert the Tx_DIS Pin to full Tx turn-up
RX_LOS assert time	Between RX input power below LOS threshold and RX_LOS assertion		0.1	ms	
RX_LOS de-assert time	Between RX input power above LOS threshold and RX_LOS negation		0.1	ms	
GLB_ALRM assert delay time	Between occurrence of the FAWS condition and GLB_ALRMn assertion		150	ms	
GLB_ALRM de-assert delay time	Between host clear action of FAWS latched registers and GLB_ALRMn negotiation		150	ms	
PRG_ALRM assert time	Between occurrence of the triggering condition and alarm assertion		150	ms	
PRG_ALRM de-assert time	Between end of the triggering condition and alarm negation		150	ms	

3.9 LLDP Requirements

The LLDP shall be fully compliant to [4].

- LLDP Rx shall support behaviour defined in 802.1AB section 9.2.9 and the Rx state machine.

- Support receiver side only LLDP mode on all Ethernet interface (include pure Ethernet client and OpenZR+ line interface).
  - Support per port enable/disable LLDP
- Support configurable LLDP filtering mechanism:
  - Filter by MAC DA, or
  - Filter by EthType (0x88CC) for LLDP over Ethernet (no VLAN encapsulation)

Please be noted:

- When LLDP frame being configured with both EthType and MAC destination multicast address as defined in 802.1AB - The Ethernet client mapping shall forward the frame to downstream but not terminating LLDP frames.

3.10 Performance Monitoring Management

The module shall support the performance monitor per [5,7,8] for related facility and entity performance monitor (PM). Table 20 is a summary for the PM management that the CFP2DCO module needs to cover.

Table 20 Performance Management

Description	Available
Physical	
Input power of Transceiver	Yes
Input Voltage of Transceiver	Yes
Laser Bias Current of Transceiver	No
Laser-Age in %	Yes
Output Power of Transceiver	Yes
TEC Current	No
Temperature of Transceiver	Yes
Ethernet RMON	
broadcast_pkts	Yes
crc errors	Yes
fragments	Yes
jabbers	Yes
multicast_pkts	Yes
octets	Yes
oversize_pkts	Yes
packet_trap (LLDP)	Yes
pkts	Yes
pkts_1024_to_1518_octets	Yes
pkts_128_to_255_octets	Yes

pkts_1519_to_max_octets	Yes
pkts_256_to_511_octets	Yes
pkts_512_to_1023_octets	Yes
pkts_64_octets	Yes
pkts_65_to_127_octets	Yes
undersize_pkts	Yes
OCh	
Actual Frequency of the Received Optical Signal	Yes
Carrier Frequency Offset of the Received Optical Signal	Yes
Chromatic Dispersion	Yes
Electric SNR	Yes
EVM	No
OSNR	Yes
Polarization Dependent Loss	Yes
Post-FEC BER	No
Pre-FEC BER	Yes
Pre-FEC Threshold	Yes
Q-Factor	Yes
Differential Group Delay	Yes
Second Order Polarization Mode Dispersion	Yes
State of Polarization	Yes
Total Number of FEC Corrected Bits	Yes
Total Number of FEC Corrected Bytes	No
Total Number of FEC Uncorrectable Blocks/Codewords	Yes

3.11 Fault Management

The module shall support fault management items described in this section and follow the definition in [7].

Table 21: Fault Management List

Description	Available
Physical	
Alarm Indicating DSP Failure	Yes
Alarm Module Temperature Higher than Threshold	Yes
Laser Failure	Yes

Input Power Lower than Threshold	Yes
Input Power Higher than Threshold	Yes
Output Power Higher than Threshold	Yes
Output Power Lower than Threshold	Yes
SW Failure	Yes
Temperature Over Limit	Yes
Transmitter Failure	Yes
Ethernet	
Local Fault on Ethernet Rx	Yes
Local Fault on Ethernet Tx	Yes
Loss of Synchronization on Ethernet Rx	Yes
Remote Fault on Ethernet Rx	Yes
Remote Fault on Ethernet Tx	Yes
Rx Ethernet High BER	Yes
Rx LOS SYNC	Yes
Rx PCS Error	Yes
Rx LOS (Client)	Yes
Signal Degrade CRC Error	Yes
Signal Degrade PCS Error	Yes
Total number of BIP errors at PCS	Yes
Tx LOS SYNC	Yes
OCh	
PreFEC Degrade	Yes
PreFEC High BER	Yes
PostFEC Degrade	Yes
ODUCn	
AIS	Yes **[GL2]**
BDI	Yes **[GL2]**
BEI	Yes **[GL2]**
Background Block Errors	Yes **[GL2]**
Code Violations	Yes **[GL2]**
Errored Seconds	Yes **[GL2]**
Errored Blocks	Yes **[GL2]**
LCK	Yes **[GL2]**

OCI	Yes **[GL2]**
Severely Errored Seconds	Yes **[GL2]**
Signal Degrade	Yes **[GL2]**
TIM	Yes **[GL2]**
Unavailable Seconds	Yes **[GL2]**
ODUk/ODUflex	
AIS	Yes **[GL2]**
Background Block Errors	Yes **[GL2]**
BDI	Yes **[GL2]**
BEI	Yes **[GL2]**
Code Violations	Yes **[GL2]**
Errored Seconds	Yes **[GL2]**
Errored Blocks	Yes **[GL2]**
LCK	Yes **[GL2]**
LOFLOM	Yes **[GL2]**
OCI	Yes **[GL2]**
Signal Degrade	Yes **[GL2]**
Severely Errored Seconds	Yes **[GL2]**
TIM	Yes **[GL2]**
Unavailable Seconds	Yes **[GL2]**
OTUCn	
AIS	Yes **[GL2]**
Background Block Errors	Yes **[GL2]**
BDI	Yes **[GL2]**
Code Violations	Yes **[GL2]**
Errored Blocks	Yes **[GL2]**
Errored Seconds	Yes **[GL2]**
LOF	Yes **[GL2]**
LOM	Yes **[GL2]**
Signal Degrade (DEG)	Yes **[GL2]**
Severely Errored Seconds	Yes **[GL2]**
Signal Failure	Yes **[GL2]**
TIM	Yes **[GL2]**
Unavailable Seconds	Yes **[GL2]**

The module shall support standard maintenance signal behaviour for fault management, as defined by [2,5,7,8].

Please be noted for Ethernet client egress direction, the module shall support configurable option of whether insert LF or Idle as maintenance signal during server layer failure (SSF). The Idle signal is for the consideration of reduce the traffic interruption time during line side protection switch event, i.e. the OTS, OMS or OCH protection.

3.12 Path Monitoring Management [GL2]

The module shall

- fully compliant to [5,6] in the definition of trail trace identifier (TTI) process and configuration on SAPI, DAP and OPER.
- support delay measurement on ODUk, ODUflex and ODUCn in both remote end loopback mode and remote end DM bit stream loopback mode as described in [7].

3.13 Test Signals

The module shall support:

- Framed PRBS test signal on network/line interface by replace openZR+ or FlexO **[GL2]** payload with PRBS7, PRBS11, PRBS15, PRBS23, PRBS31 patterns.
- OPUCn payload PRBS test signal for line interface test and diagnosis **[GL2]**.
- OPUk/OPUflex payload PRBS test signal, independently for each host interface **[GL2]**.
- Framed PRBS test signal on host/client interface by replace 100GBE, 400GBE payload with PRBS7, PRBS15, PRBS23, PRBS31 patterns.
- Client-side PCS Idle test signal, independently for each host interface
- Framed PRBS and NULL test signal on ODU container layer **[GL2]**.
- Delay Measurement (DM) on ODU container layer **[GL2]**.
- Specific test pattern generation and monitor on client SerDes for 100/200/400G Ethernet interface as per IEEE 802.3-2018:
  - PAM4 Signalling:
    - PRBS31Q, PRBS13Q,
  - NRZ Signalling:
    - PRBS31, PRBS9,

  All PRBS signals are unframed and shall support both inverted and non-inverted mode.
- Eye Scan and PRBS checker for BER reporting on client SerDes that is compliant to client Test Point TP4.

3.14 Loopbacks

The module shall

- Support various loopbacks as given in Figure 1, where Rx terminal loopback & Tx facility loopback will be supported in **[GL2]**.

3.15 3R Regeneration

Support 3R regeneration through Rx PCS Loopback for GL1 version.

Support 3R regeneration through CFP2-DCO line interface loopback at ODUCn layer **[GL2]**.

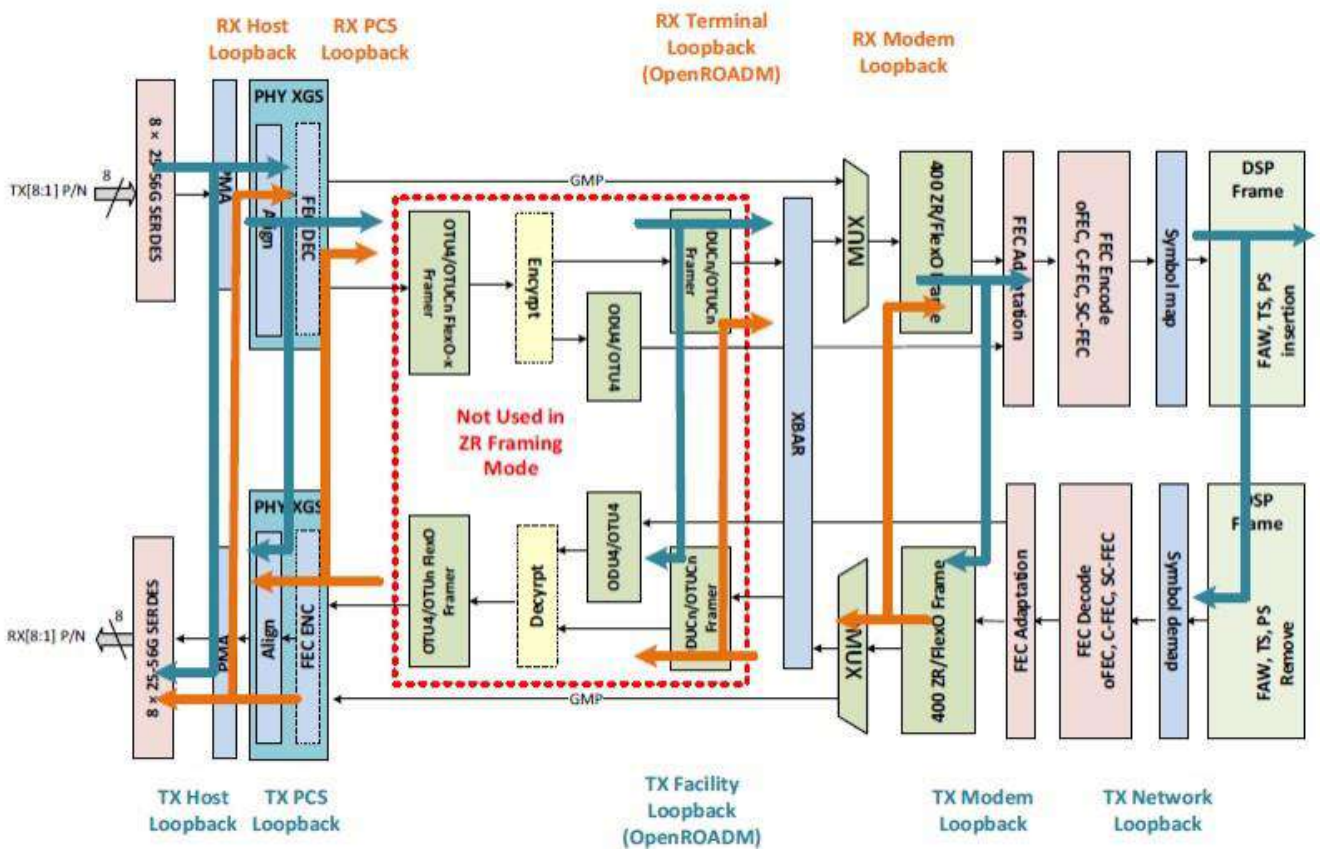

Figure 1: Loopback types

3.16 Miscellaneous

- Support automatic hitless PCS idle insertion for configurable duration when service interruption happens.
- Support service interruption time report.
- Support hitless FW upgrade in-service.
- Support fast consequent action per pre-FEC BER cross pin driving (DCO pin 37).
- Support fast BER monitoring and fast propagation through PCS local SD insertion.
- Support 1s PM interval and reliable scheme for PM data (counter and gauge) synchronization every 1s.
- Support configurable CD range.
- Support the insertion of LF, RF and PCS Idle from both client to line direction and line to client direction.
- Support the insertion of AIS, OCI, LCK, BDI, BEI on ODUk/ODUflex and ODUCn **[GL2]**

4 PHYSICAL CHARATERISTICS

4.1 Mechanical Drawing

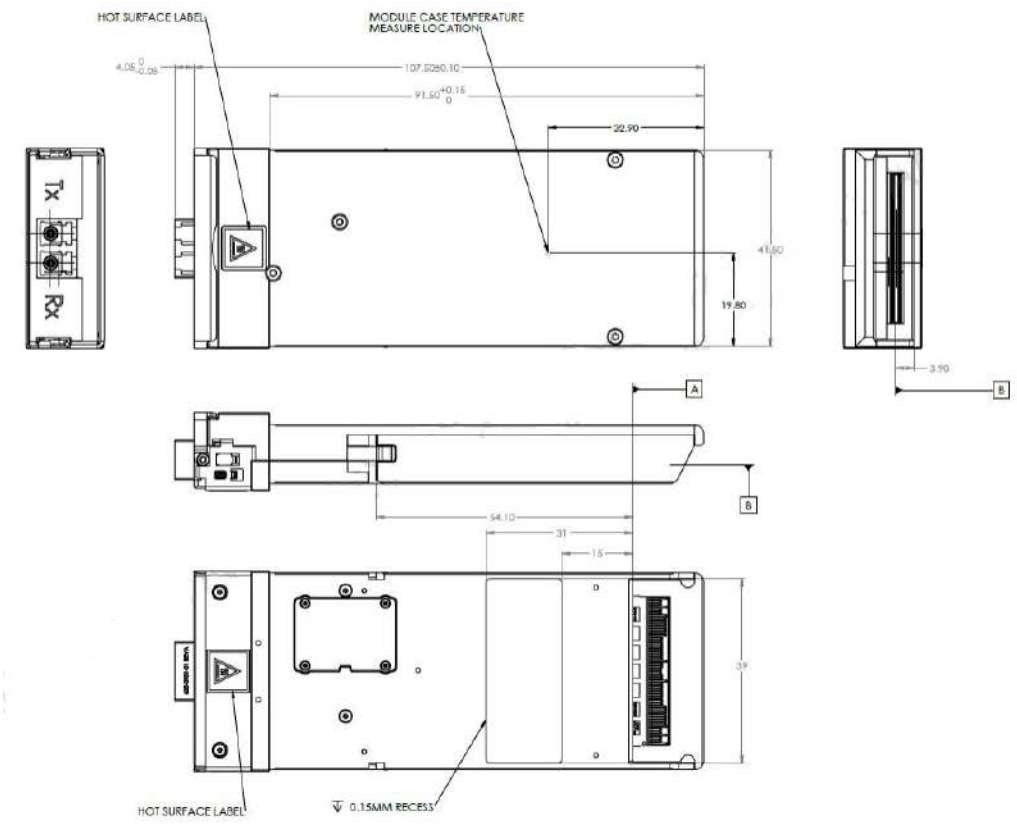

Figure 2: **Mechanical Drawing of the latch version DCO**

4.2 Module Weight

The weight of the module is 100g +/- 10g.

5 DEFAULT CONFIGURATION

The requirement for a default configuration on start-up is defined in Table 22.

Table 22: Default configuration

#	Default configuration	Values	Notes
1	Line data rate	400G	
2	Line modulation format	16QAM	
3	Line roll off (RRC)	0.2	
4	Line dispersion range	-10000…2000 ps/nm	
5	Line FEC	O-FEC	The available highest powerful FEC
6	Client signal type	100GBE	All four client ports
7	Client host interface	100GAUI-2	All four client ports
8	Client mapping	GMP	
9	HOST FEC on 100GAUI-2 (KP RS-544)	Enabled	
10	Line Tx power (dBm)	Max Tx power of the mode	Return to this default value after reset
11	Line Tx frequency	196.0875 THz	Return to this default value after reset