AQSFP28-100G-EZR4

100Gbps QSFP28 EZR4 Transceiver, 100km Reach

Product Features

- Supports 100GBASE 100GE;
- Lane bit rate 25.78 Gb/s 100GE
- Up to 100km transmission on SMF;
- LAN WDM laser and PIN receiver with SOA;
- Support Multi-Pin function with IntL/RxLOSL and LPMode/TxDIS;
- High speed I/O electrical interface (CAUI-4);
- I2C interface with integrated Digital Diagnostic monitoring;
- QSFP28 MSA package with duplex LC connector;
- Single +3.3V power supply;
- Typical power consumption 6.5 W;
- Operating case temperature: 0 to +70 ° C;
- Compliant to IEEE 802.3bm and ITU-T G.959;
- Compliant to SFF-8636 and SFF-8679;
- Complies with EU Directive 2015/863/EU;

Applications

- 100GBASE-ZR4 plus;

Absolute Maximum Ratings

It has to be noted that the operation in excess of any individual absolute maximum ratings might cause permanent damage to this module.

Parameter	Symbol	Min	Max	Unit	Notes
Storage Temperature	T_S	-40	+85	℃	
Power Supply Voltage	V_{CC}	-0.5	+4.0	V	
Operating Relative Humidity	RH	-	+85	%	

Recommended Operating Conditions

Parameter	Symbol	Min.	Typical	Max.	Unit	Notes
Operating Case Temperature	T_C	0	-	+70	℃	
Power Supply Voltage	V_{CC}	3.13	3.3	3.47	V	
Power Supply Current	I_{CC}	-	-	1.97	A	
Typical Power Dissipation	P_D	-	-	6.5	W	
Aggregate Bit Rate	BR_{AVE}	-	103.125	-	Gb/s	
Lane Bit Rate	BR_{LANE}	-	25.78	-	Gb/s	
Transmission Distance	TD	-	-	100	km	Over SMF

Optical Characteristics

Transmitter						
Parameter	**Symbol**	**Min.**	**Typical**	**Max.**	**Unit**	**Notes**
Center Wavelength Lane 0	λ_0	1294.53	1295.56	1296.59	nm	
Center Wavelength Lane 1	λ_1	1299.02	1300.05	1301.09	nm	
Center Wavelength Lane 2	λ_2	1303.54	1304.58	1305.63	nm	
Center Wavelength Lane 3	λ_3	1308.09	1309.14	1310.19	nm	
Total Launch Power, 100GE	P_{ALL}	-	-	14	dBm	1
Average Launch Power per Lane, 100GE	P_{TX_LANE}	4	-	8	dBm	1
Difference in launch power between lanes	$P_{TX\_Delta\_LANE}$	-	-	3.6	dB	
Average Output Power (Laser Turn off)	$P_{0UT-OFF}$	-	-	-30	dBm	
Side Mode Suppression Ratio	SMSR	30	-	-	dB	
Extinction Ratio, 100GE	ER	6	-	-	dB	
Optical Eye Mask	IEEE 802.3 {0.25,0.4, 0.45, 0.25, 0.28, 0.4}					
Receiver						
Center Wavelength Lane 0	λ_0	1294.53	1295.56	1296.59	nm	
Center Wavelength Lane 1	λ_1	1299.02	1300.05	1301.09	nm	
Center Wavelength Lane 2	λ_2	1303.54	1304.58	1305.63	nm	
Center Wavelength Lane 3	λ_3	1308.09	1309.14	1310.19	nm	
Damage threshold	Pdamage	5.5	-	-	dBm	
Average Rx Power per Lane, 100GE	P_{Rx_LANe}	-30	-	4.5	dBm	2
Difference in launch power between lanes	$P_{RX\_Delta\_LANE}$	-	-	4.5	dB	
Los Assert	LosA	-40	-	-	dBm	
Los De-assert	LosDA	-	-	-31	dBm	
Los Hysteresis	LosH	0.5	-	5	dB	

Note:
1. The optical power is launched into SMF.
2. Measured with a PRBS 231-1 test pattern @25.78125 Gb/s, BER≤5E-5.

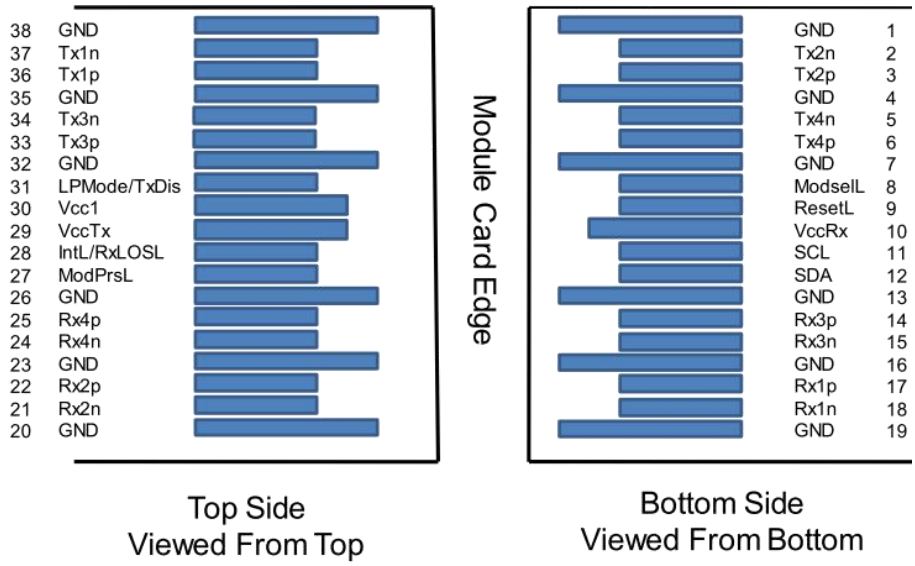
Electrical Characteristics

High-Speed Signal: Compliant to CAUI-4 (IEEE 802.3bm)

Low-Speed Signal: Compliant to SFF-8679.

Transmitter (Module Input)						
Parameter	**Symbol**	**Min.**	**Typical**	**Max.**	**Unit**	**Notes**
Differential Data Input Amplitude	$V_{IN,P-P}$	85	-	900	mVpp	
Differential Termination Mismatch		-	-	10	%	
Differential input return loss(min)	RLd(f)	Compliance with IEEE802.3ba Equation (83A－5)			dB	
Differential to common mode input return loss (min)	RLdc(f)	Compliance with IEEE802.3ba Equation (83A－6)			dB	
LPMode, Reset and ModSelL, V in low	V_{IL}	-0.3	-	0.8	V	
LPMode, Reset and ModSelL, V in high	V_{IH}	2.0	-	VCC+0.3	V	
Receiver (Module Output)						
Differential Data Output Amplitude	$V_{OUT,P-P}$	200	-	900	mVpp	
Differential Termination Mismatch（1MHZ）		-	-	10	%	
Transition time, 20% to 80%	Tr Tf	12	-	-	ps	
Differential output return loss (min)	RLd(f)	Compliance with IEEE802.3ba Equation (83A－7)			dB	
Common to differential mode conversion return loss (min)	RLdc(f)	Compliance with IEEE802.3ba Equation (83A－8)			dB	
ModPrsL and IntL, V out low	V_{OL}	0	-	0.4	V	
ModPrsL and IntL, V out high	V_{OH}	VCC-0.5	-	VCC+0.3	V	

Pin Assignment



Pin Definition

PIN	Logic	Symbol	Description	Plug Seq.	Notes
1		GND	Ground	1	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	3	
3	CML-I	Tx2p	Transmitter Non-Inverted Data output	3	
4		GND	Ground	1	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	3	
6	CML-I	Tx4p	Transmitter Non-Inverted Data output	3	
7		GND	Ground	1	1
8	LVTLL-I	ModSelL	Module Select	3	
9	LVTLL-I	ResetL	Module Reset	3	
10		VccRx	+ 3.3V Power Supply Receiver	2	2
11	LVCMOS-I/O	SCL	2-Wire Serial Interface Clock	3	
12	LVCMOS-I/O	SDA	2-Wire Serial Interface Data	3	
13		GND	Ground	1	
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	3	

15	CML-O	Rx3n	Receiver Inverted Data Output	3	
16		GND	Ground	1	1
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	3	
18	CML-O	Rx1n	Receiver Inverted Data Output	3	
19		GND	Ground	1	1
20		GND	Ground	1	1
21	CML-O	Rx2n	Receiver Inverted Data Output	3	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	3	
23		GND	Ground	1	1
24	CML-O	Rx4n	Receiver Inverted Data Output	3	
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	3	
26		GND	Ground	1	1
27	LVTTL-O	ModPrsL	Module Present	3	
28	LVTTL-O	IntL/Rx_LOS	Interrupt/Rx_LOS	3	
29		VccTx	+3.3 V Power Supply transmitter	2	2
30		Vcc1	+3.3 V Power Supply	2	2
31	LVTTL-I	LPMode/TxDIS	Low Power Mode/Tx_Disable	3	
32		GND	Ground	1	1
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	3	
34	CML-I	Tx3n	Transmitter Inverted Data Output	3	
35		GND	Ground	1	1
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	3	
37	CML-I	Tx1n	Transmitter Inverted Data Output	3	
38		GND	Ground	1	1

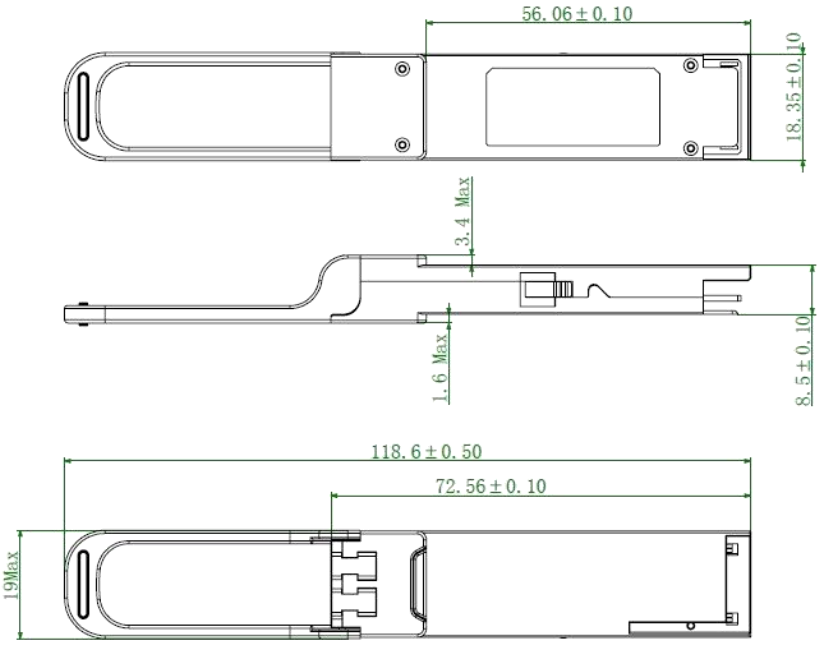
Note:
1: GND is the symbol for signal and supply (power) common for the QSFP28 module. All are common within the QSFP28 module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane.

2: Vcc Rx, Vcc1 and Vcc Tx are the receiver and transmitter power supplies and shall be applied concurrently. Requirements defined for the host side of the Host Edge Card Connector are listed in MSA. The connector pins are each rated for a maximum current of 1000 mA.

Digital Diagnostic Functions

Parameter	Range	Accuracy	Unit	Calibration
Temperature	0 to 70	±3	℃	Internal
Voltage	0 to VCC	10%	V	Internal
Tx Bias Current Per Lane	0 to 100	10%	mA	Internal
Tx Output Power Per Lane	4 to 8	±3	dBm	Internal
Rx Power (Each Lane)	-30 to 4.5	±3	dBm	Internal

Mechanical Dimensions



Ordering Information

Part Number	Product Description
AQSFP28-100G-EZR4	100Gbps QSFP28 EZR4, LWDM Wavelengths, LC Connector, 100km Reach, with DDM

ESD

This transceiver is specified as ESD threshold 1kV for high speed data pins and 2kV for all others electrical input pins, tested per MIL-STD-883, Method 3015.4 /JESD22- A114-A (HBM). However, normal ESD precautions are still required during the handling of this module. This transceiver is shipped in ESD protective packaging. It should be removed from the packaging and handled only in an ESD protected environment.